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MS-7418 (MS-6496)

Version 2.1

CPU:

Intel Dimondville

System Chipset:

Intel 945GC (North Bridge)

Intel ICH7(South Bridge)

On Board Chipset:

BIOS -- SPI

HD AUDIO CODEC(ALC888)

LAN -- Realtek RTL8111C

Clock Generator - ICS954119

Main Memory:

DDR II SO-DIMM x 1 (Max 2GB)


CF Card Connector for flash Memory

Expansion Slots:

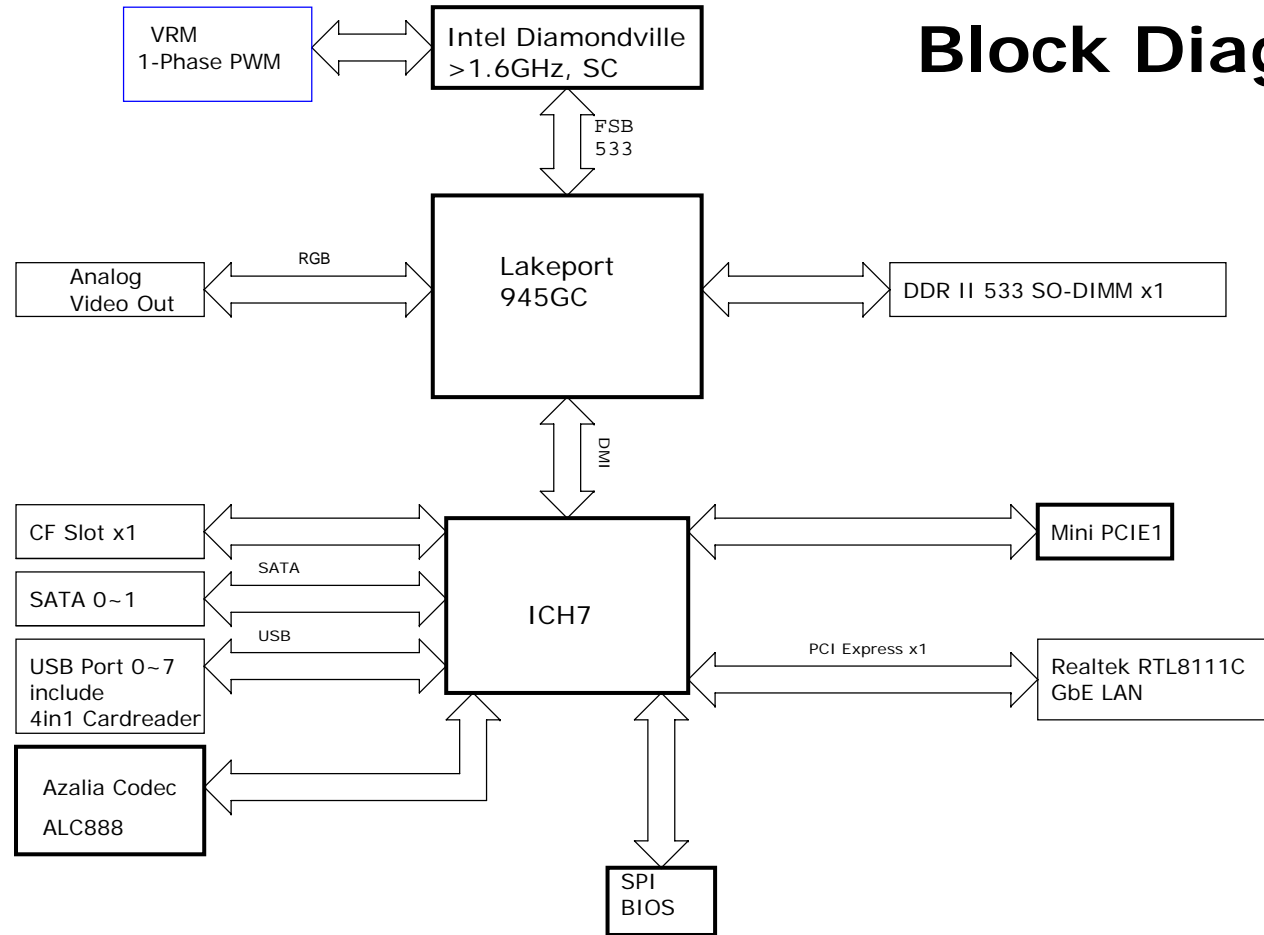
Internal Mini PCIE x1

Intersil PWM:

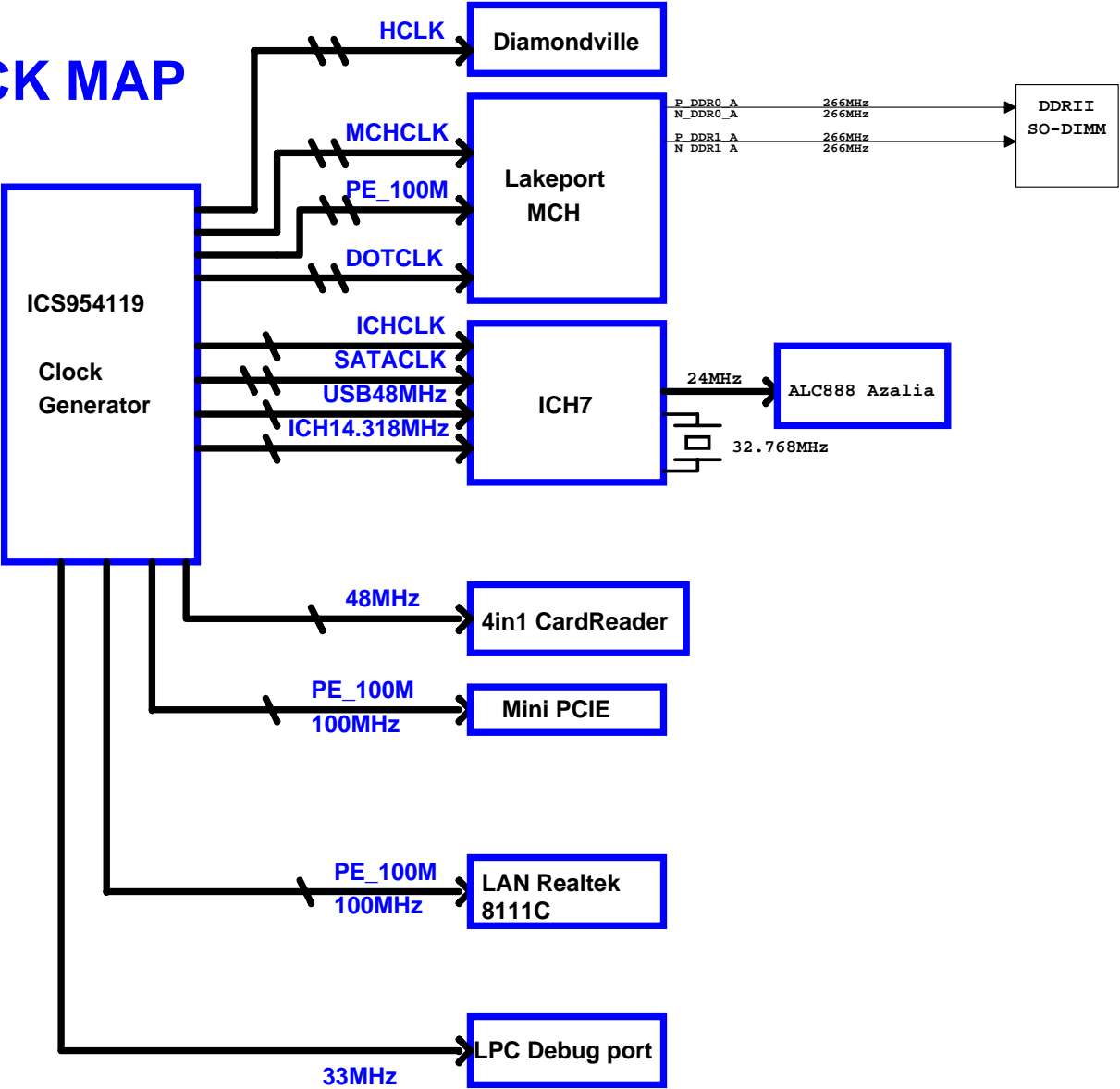
Controller: 6314

| | | | |
|---|----------------------------|-----------------------------------|------------|
|  | | MICRO-STAR INT'L CO., LTD. | |
| Title COVER SHEET | | | |
| Size | Document Number MS-7418 | | Rev 2.1 |
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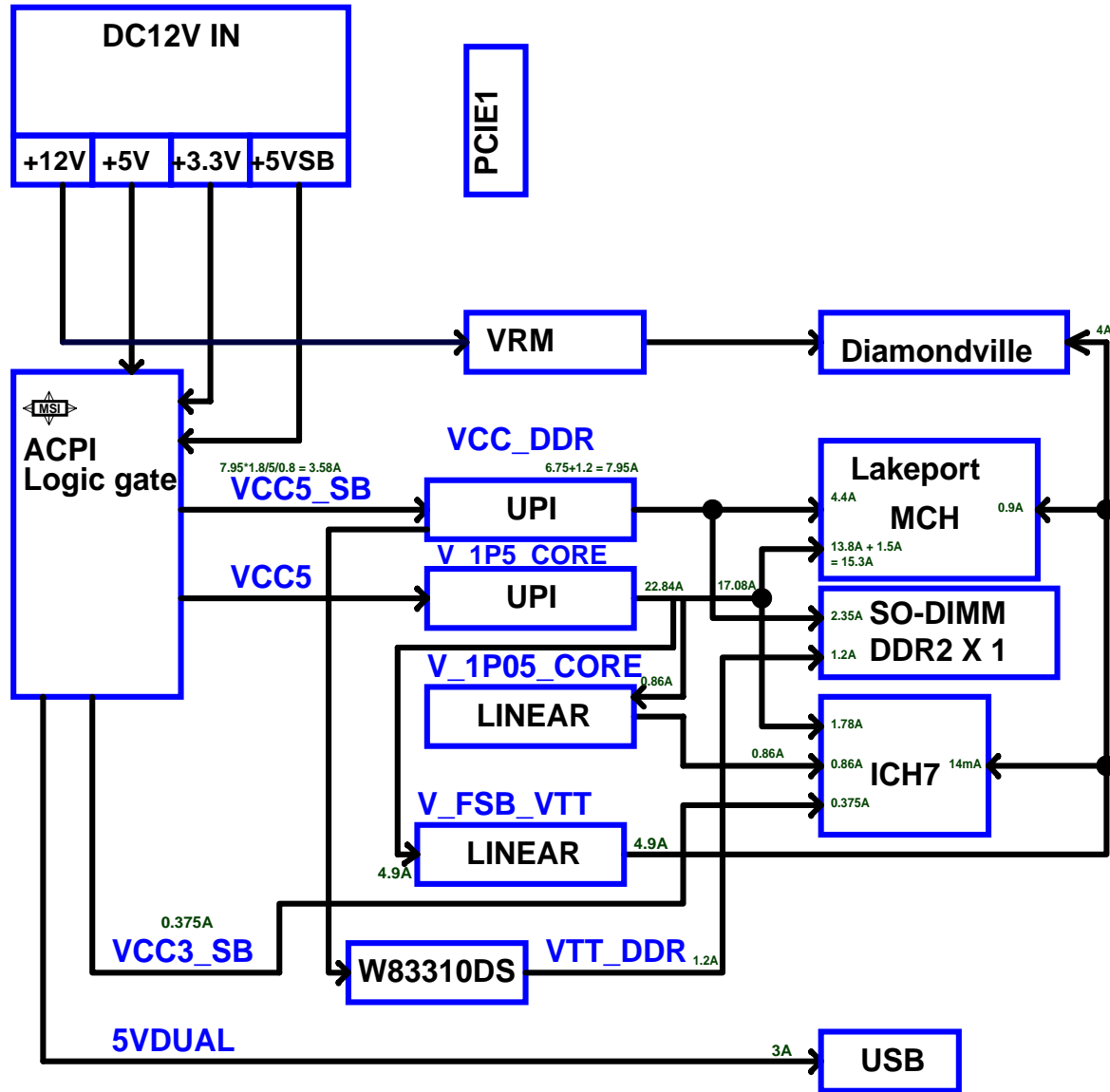
Block Diagram



CLOCK MAP



POWER MAP



ICH7

| GPIO | Alt Func | Pin | I/O/NC | Power | PU | SMI | Tol | Default | Signal Name or status |
|---|---------------|------|--------|-----------|----|-----|-----|-----------|----------------------------------|
| GPIO[0] | SIO_SMI# | AB18 | I/O | Vcc3p3 | N | Y | 5 | Input | pull high VCC3 |
| GPIO[1] | PCIREQ[5]# | C8 | I/O | V5REF | N | Y | 5 | Input | PREQ#5 |
| GPIO[2] | PIRQE# | G8 | I/OD | V5REF | N | Y | 5 | Input | PIRQ#E |
| GPIO[3] | PIRQF# | F7 | I/OD | V5REF | N | Y | 5 | Input | PIRQ#F |
| GPIO[4] | PIRQG# | F8 | I/OD | V5REF | N | Y | 5 | Input | PIRQ#G |
| GPIO[5] | PIRQH# | G7 | I/OD | V5REF | N | Y | 5 | Input | PIRQ#H |
| GPIO[6] | ATADET0 | AC21 | I/O | Vcc3p3 | N | Y | 3.3 | Input | ATADET0 |
| GPIO[7] | GPI7 | AC18 | I/O | Vcc3p3 | N | Y | 3.3 | Input | pull high VCC3 |
| GPIO[8] | SIO_PME# | E21 | I/O | VccSus3p3 | N | Y | 3.3 | Input | SIO_PME# pull high VCC3_SB |
| GPIO[9] | WLAN_PWRON | E20 | I/O | VccSus3p3 | N | Y | 3.3 | Output | pull high VCC3_SB |
| GPIO[10] | unmuxed | A20 | I/O | VccSus3p3 | N | Y | 3.3 | Input | pull high VCC3_SB |
| GPIO[11] | SMBALERT# | B23 | I/O | VccSus3p3 | N | Y | 3.3 | Input | pull high VCC3_SB |
| GPIO[12] | unmuxed | F19 | I/O | VccSus3p3 | N | Y | 3.3 | Input | pull high VCC3_SB |
| GPIO[13] | unmuxed | E19 | I/O | VccSus3p3 | N | Y | 3.3 | Input | pull high VCC3_SB |
| GPIO[14] | ADT7467_ALERT | R4 | I/O | VccSus3p3 | N | Y | 3.3 | Input | pull high VCC3_SB |
| GPIO[15] | unmuxed | E22 | I/O | VccSus3p3 | N | Y | 3.3 | Input | pull high VCC3_SB |
| GPIO[16] | unmuxed | AC22 | I/O | Vcc3p3 | N | N | 3.3 | 0 | NC |
| GPIO[17] | PCIGNT[5]# | D8 | I/O | Vcc3p3 | N | N | 3.3 | N/A | NC |
| GPIO[18] | unmuxed | AC20 | I/O | Vcc3p3 | N | N | 3.3 | 1 | NC |
| GPIO[19] | SATA1GP | AH18 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[20] | unmuxed | AF21 | I/O | Vcc3p3 | N | N | 3.3 | 1 | NC |
| GPIO[21] | SATA0GP | AF19 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[22] | PCIREQ[4]# | A13 | I/O | Vcc3p3 | N | N | 3.3 | Input | PREQ#4 |
| GPIO[23] | LDRQ1# | AA5 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[24] | unmuxed | R3 | I/O | VccSus3p3 | N | N | 3.3 | No Change | NC |
| GPIO[25] | S1_3_LED | D20 | I/O | VccSus3p3 | Y | N | 3.3 | 1 | pull high VCC3 SB |
| GPIO[26] | unmuxed | A21 | I/O | VccSus3p3 | N | N | 3.3 | 0 | NC |
| GPIO[27] | unmuxed | B21 | I/O | VccSus3p3 | N | N | 3.3 | 0 | NC |
| GPIO[28] | unmuxed | E23 | I/O | VccSus3p3 | N | N | 3.3 | 0 | NC |
| GPIO[29] | OC#2 | C3 | I/O | VccSus3p3 | N | N | 3.3 | Input | OC#5 |
| GPIO[30] | OC#2 | A2 | I/O | VccSus3p3 | N | N | 3.3 | Input | OC#6 |
| GPIO[31] | OC#2 | B3 | I/O | VccSus3p3 | N | N | 3.3 | Input | OC#7 |
| GPIO[32] | CLEAR_CMOS# | AG18 | I/O | Vcc3p3 | N | N | 3.3 | 1 | CLEAR_CMOS#, ONLY pull high VCC3 |
| GPIO[33] | unmuxed | AC19 | I/O | Vcc3p3 | N | N | 3.3 | 1 | NC |
| GPIO[34] | unmuxed | U2 | I/O | Vcc3p3 | N | N | 3.3 | 0 | NC |
| GPIO[35] | unmuxed | AD21 | I/O | Vcc3p3 | N | N | 3.3 | 1 | NC |
| GPIO[36] | SATA2GP | AH19 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[37] | SATA3GP | AE19 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[38] | unmuxed | AD20 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[39] | unmuxed | AE20 | I/O | Vcc3p3 | N | N | 3.3 | Input | pull high VCC3 |
| GPIO[48] | GNT4# | A14 | I/O | Vcc3p3 | N | N | 3.3 | N/A | GNT4# |
| GPIO[49] | CPUPWRGD | AG24 | I/O | V_CPU_IO | N | N | CPU | N/A | H_PWRGD |
| GPI[15..0] can configured to cause a SMI# or SCI. | | | | | | | | | |

Following are the GPIOs that need to be terminated properly if not used:
GPIO[39;36;23;21;19;7;0]: default as inputs and should be pulled up to Vcc3_3 if unused.
GPIO[31;29;15;8]: default as inputs and should be pulled up to VccSus3_3 if unused.

| FWH Note: FWH GPs should only be used for static options, do not put dynamic nets on these | | | | |
|---|------|-------|-----|-------------|
| GPIO | Pin# | Power | Tol | Signal Name |
| FPGI[0] | 6 | Main | 3.3 | pull-down |
| FPGI[1] | 5 | Main | 3.3 | pull-down |
| FPGI[2] | 4 | Main | 3.3 | pull-down |
| FPGI[3] | 3 | Main | 3.3 | pull-down |
| FPGI[4] | 30 | Main | 3.3 | pull-down |

| SIGNAL | DEVICE |
|--------------|----------------|
| MiniPCleRST# | MINI PCIE SLOT |
| TPMRST# | TPM |
| LANRST# | LAN 8111C |
| PCIRST_ICH7# | BUFFER IC |
| CF_RST# | CF_CARD |
| H_CPURST# | CPU |
| FWHRST# | LPT Debug port |
| MCHRST# | MCH |

SMBCLK, SMBDATA, DDR2, PCIEX1, CLKGEN, ICH7, ADT7464

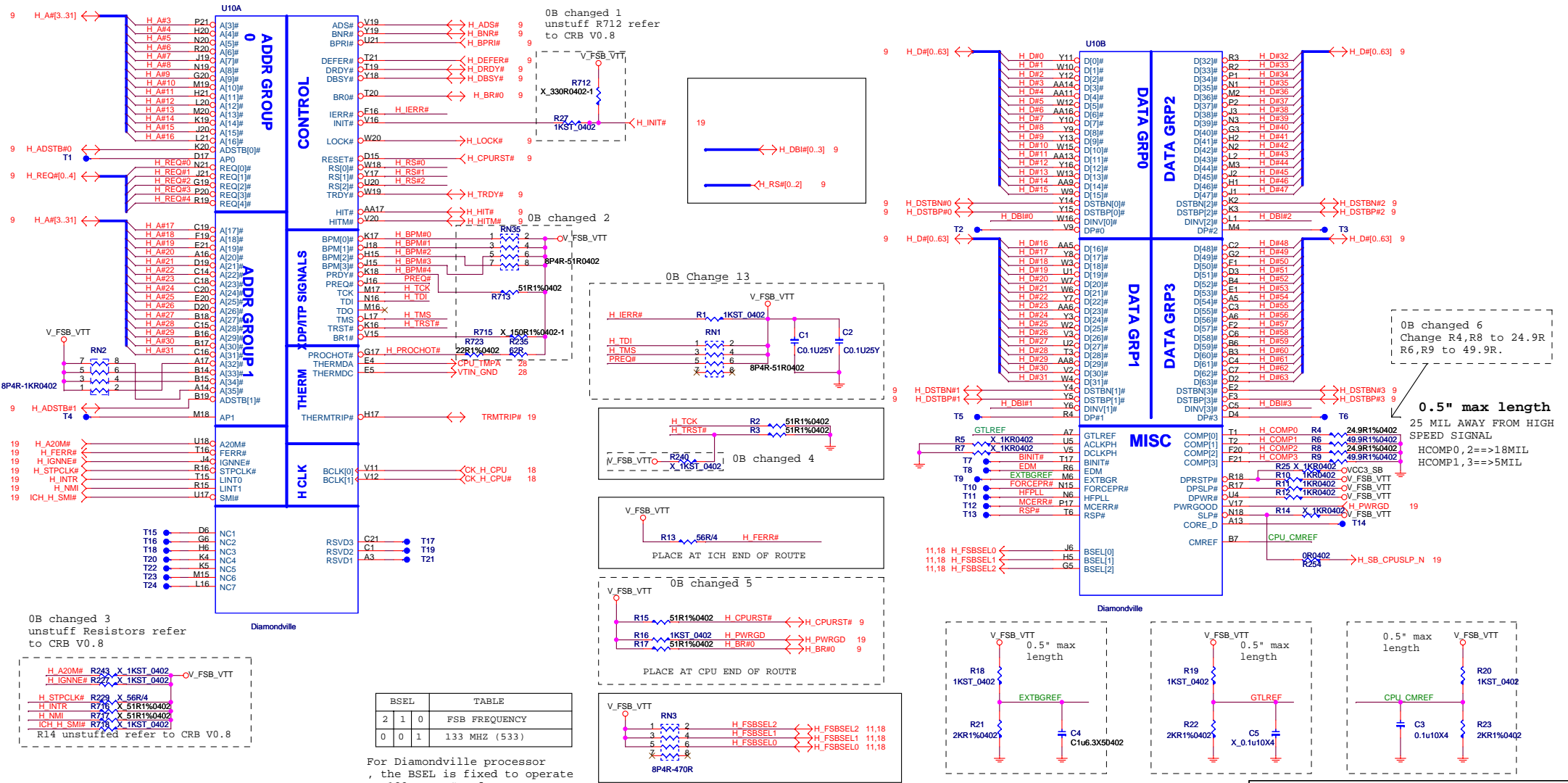
DDRII DIMM Config.

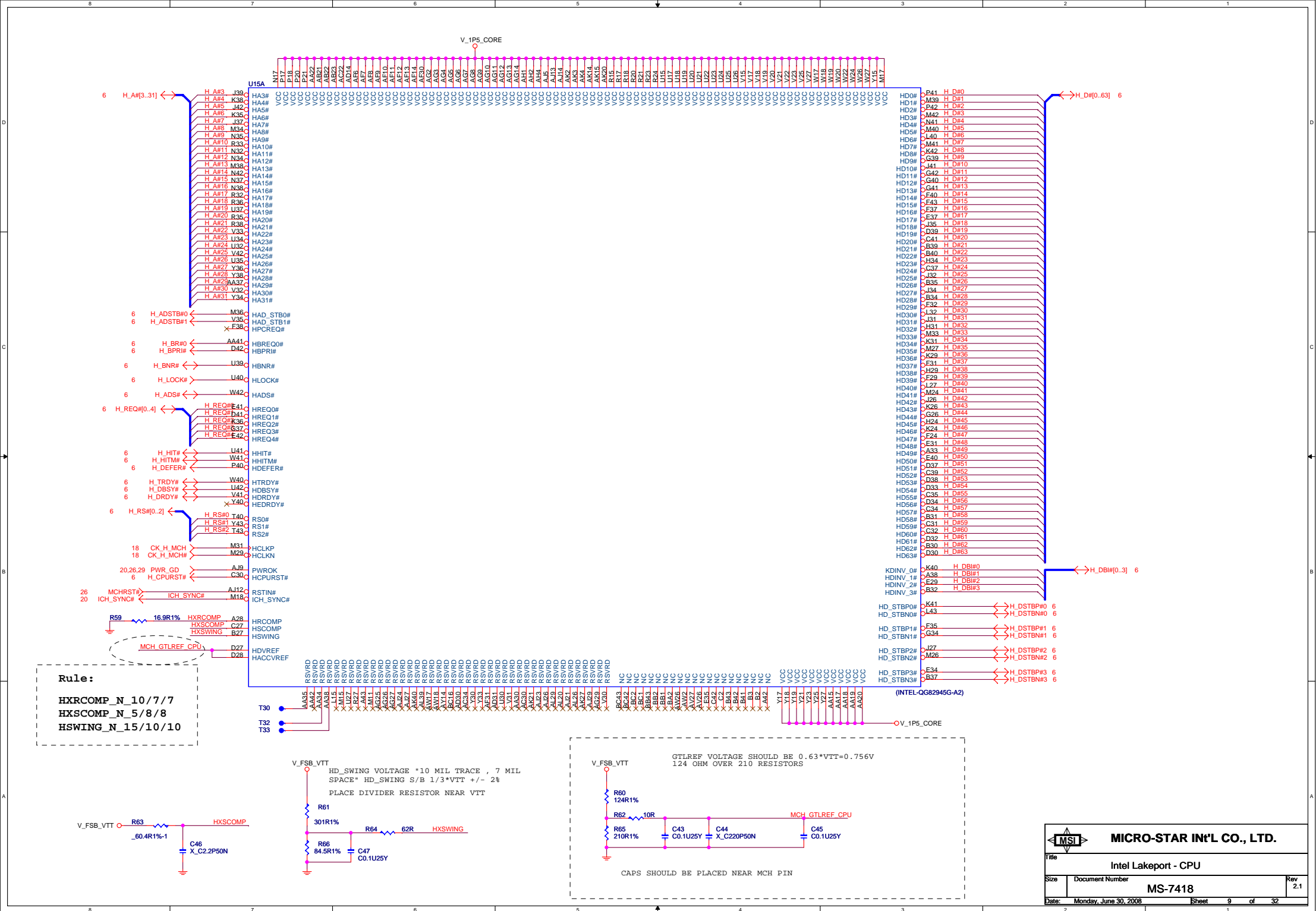
| DEVICE | ADDRESS | CLOCK |
|--------|---------|--|
| DIMM 1 | A0H | MCLK_A0/MCLK_A#0 MCLK_A1/MCLK_A#1 MCLK_A2/MCLK_A#2 |

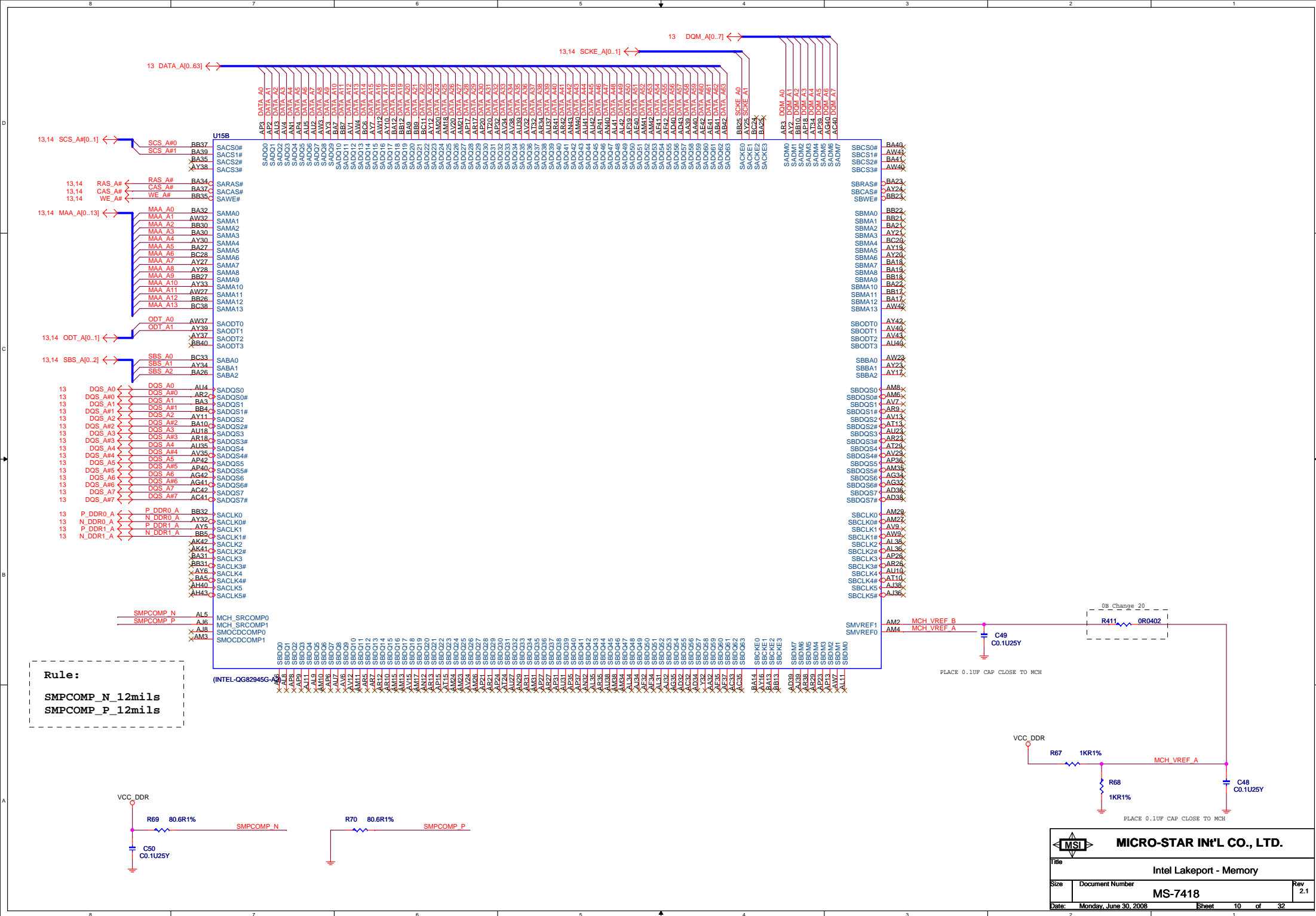
JUMPER SETTING

| | | |
|--------------|-------------|------------|
| JBAT1 | (1-2)NORMAL | (2-3)CLEAR |
|--------------|-------------|------------|

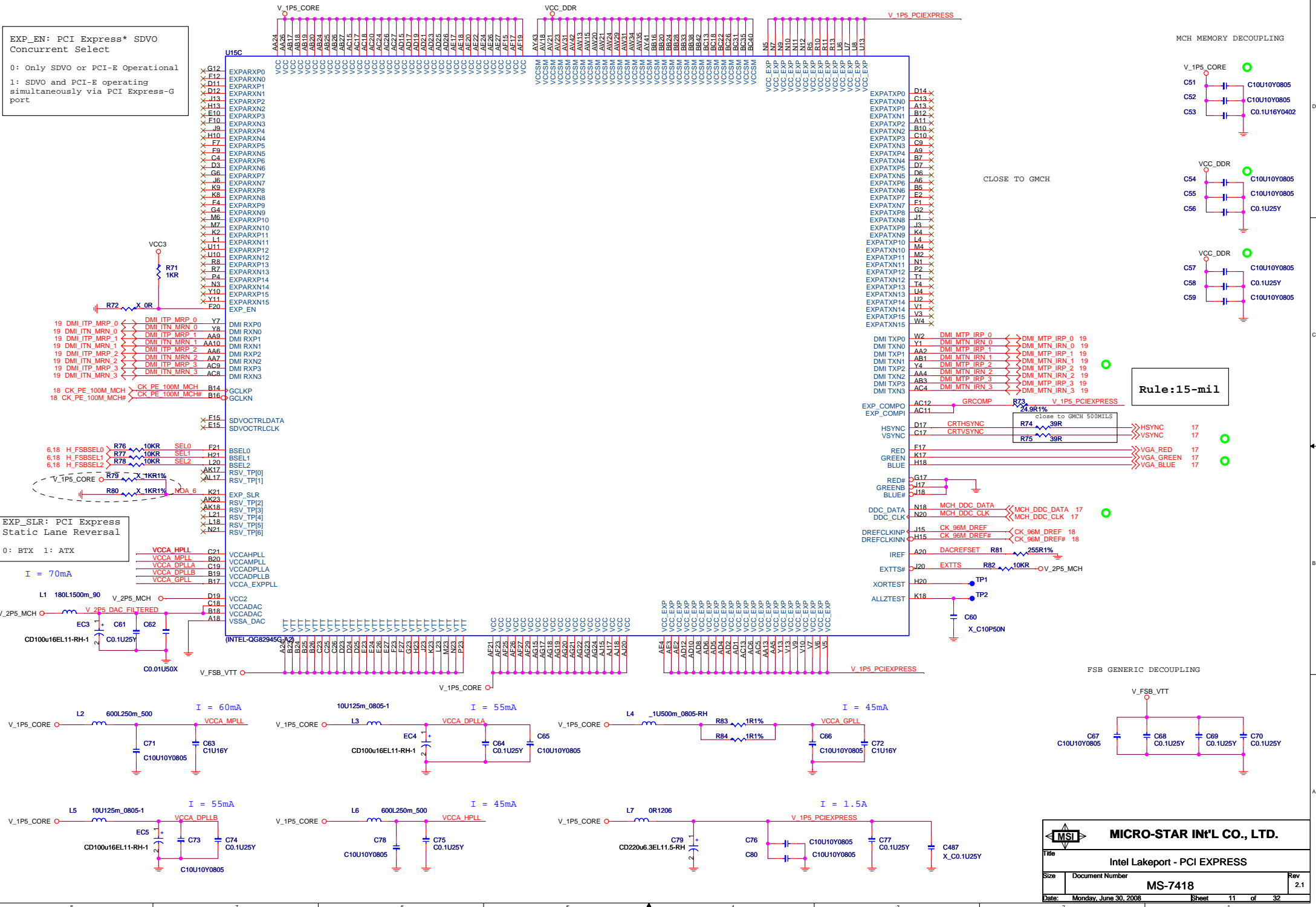
CPU SIGNAL BLOCK

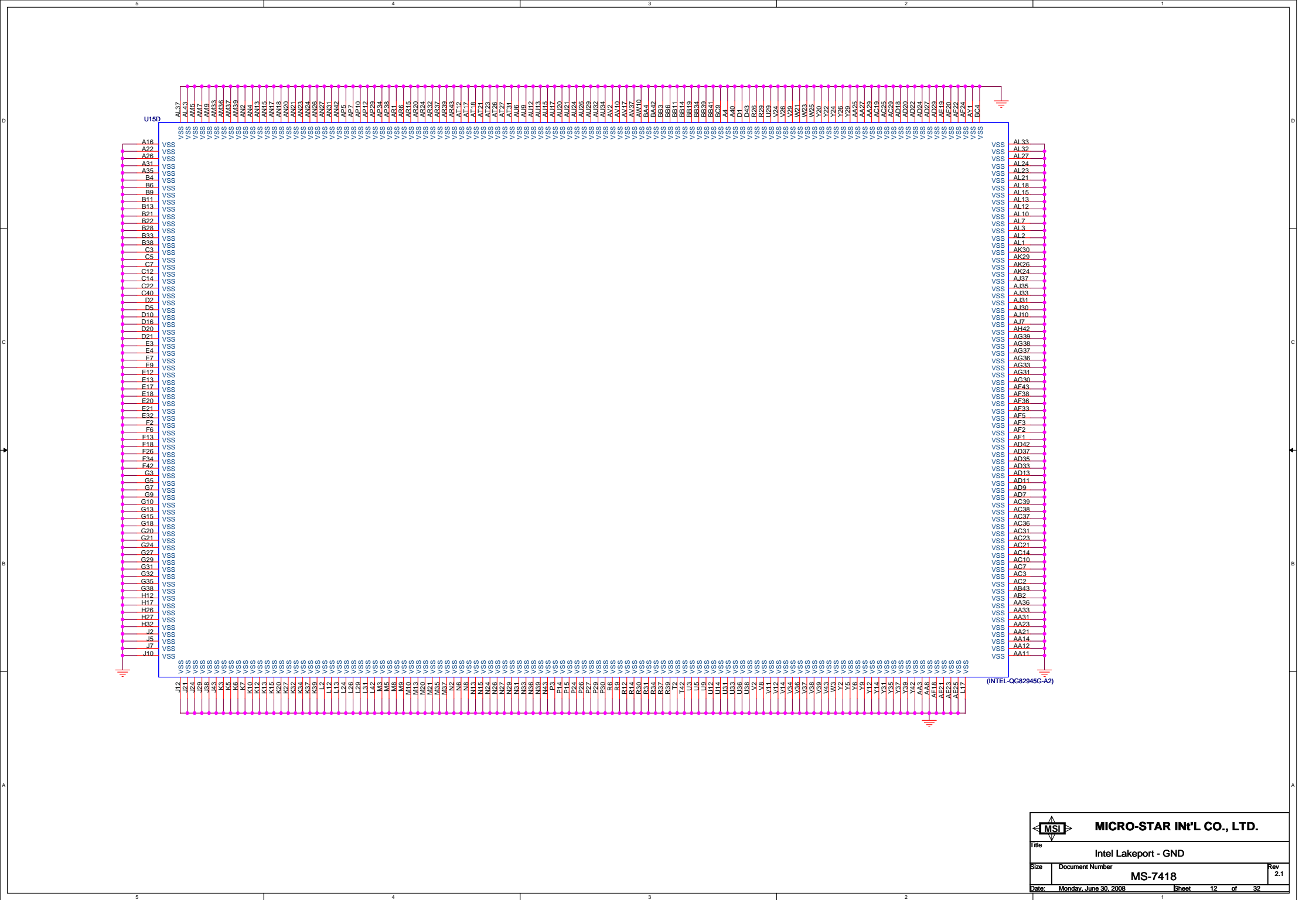




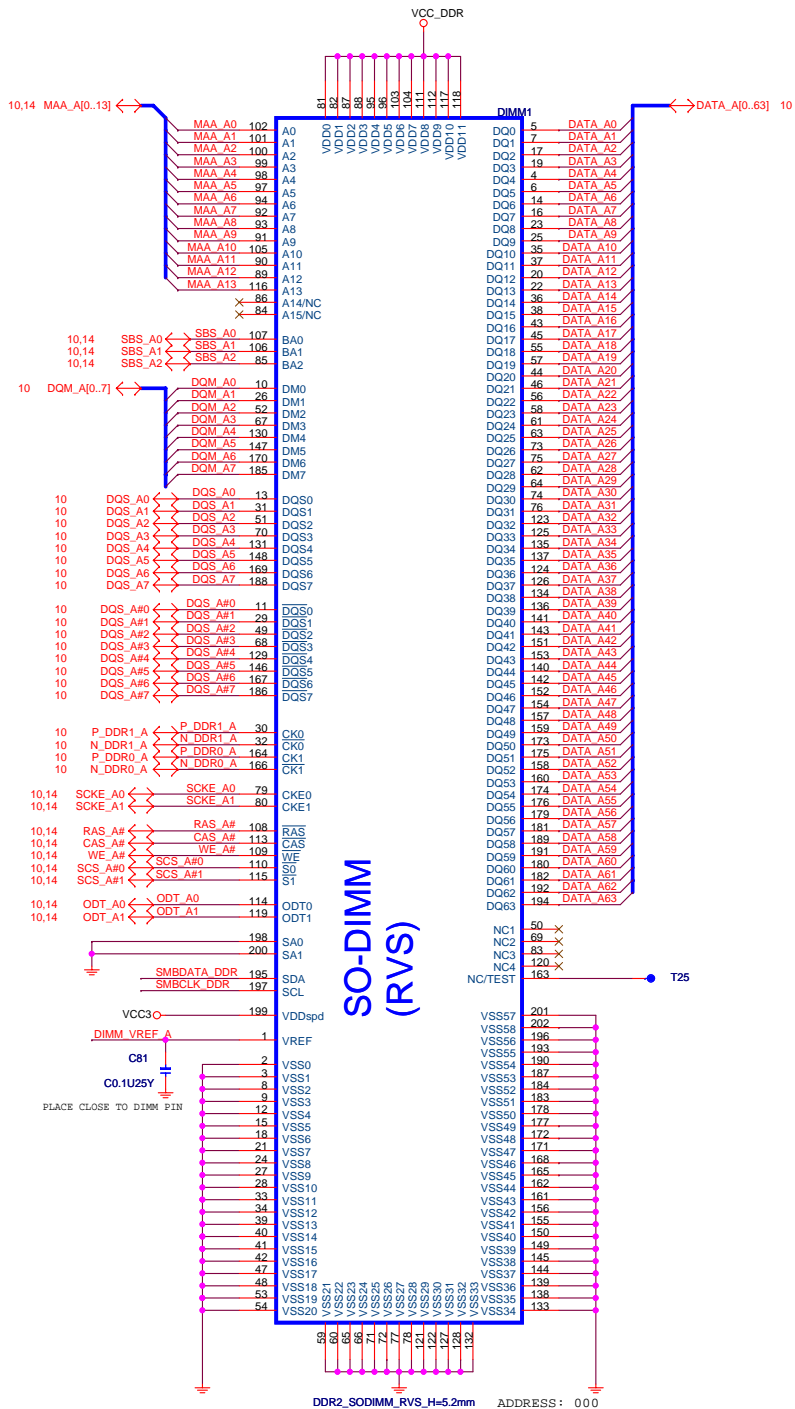


```
0: Only SDVO or PCI-E Operational
1: SDVO and PCI-E operating
simultaneously via PCI Express-G
port
```



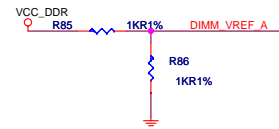


DDR2 SO-DIMM

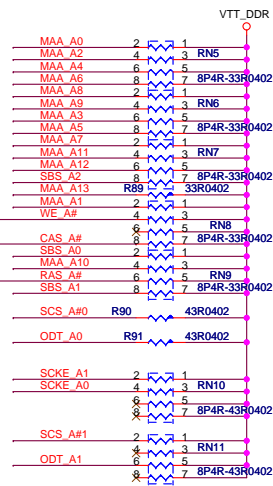
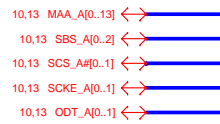
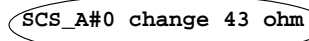
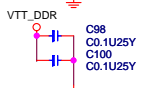
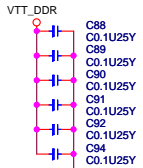
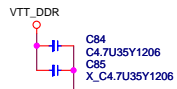
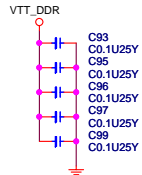
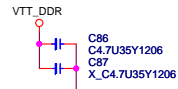
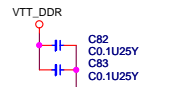
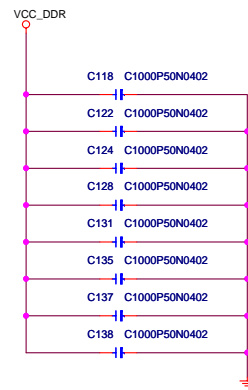
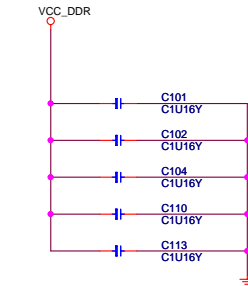
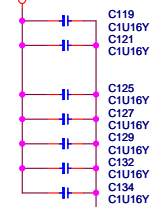
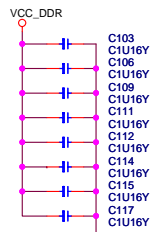
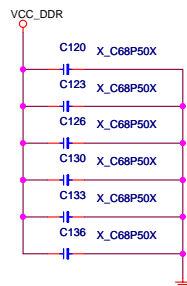
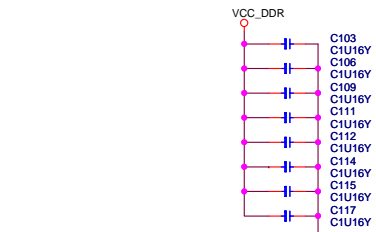
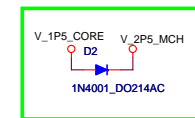


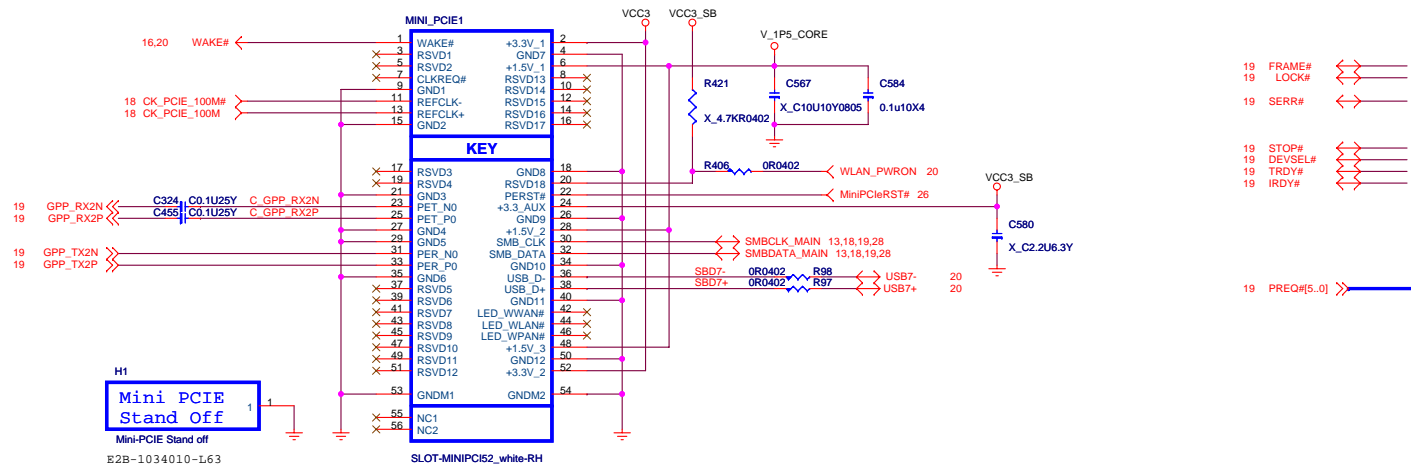
DDR2_SODIMM_RVS_H=5.2mm

ADDRESS: 000

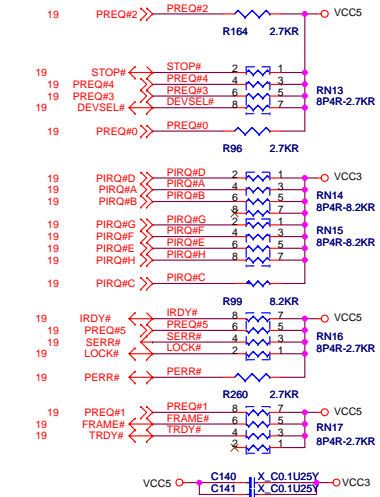


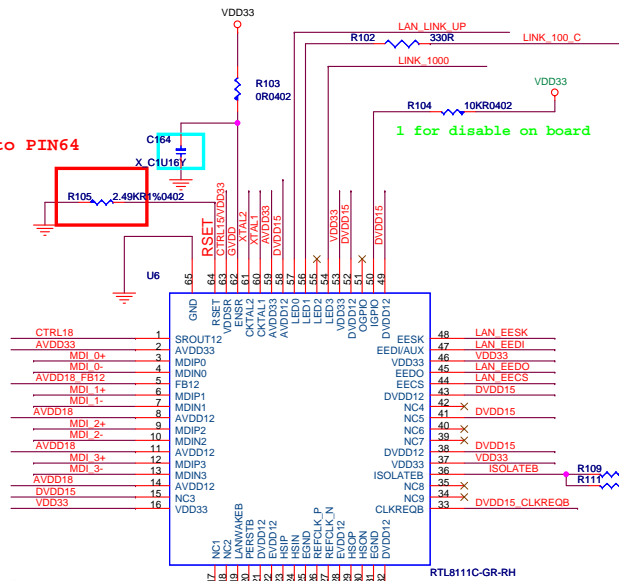
CHANNEL B V_SM_VTT
DECOUPLING CAPS

[illegible]



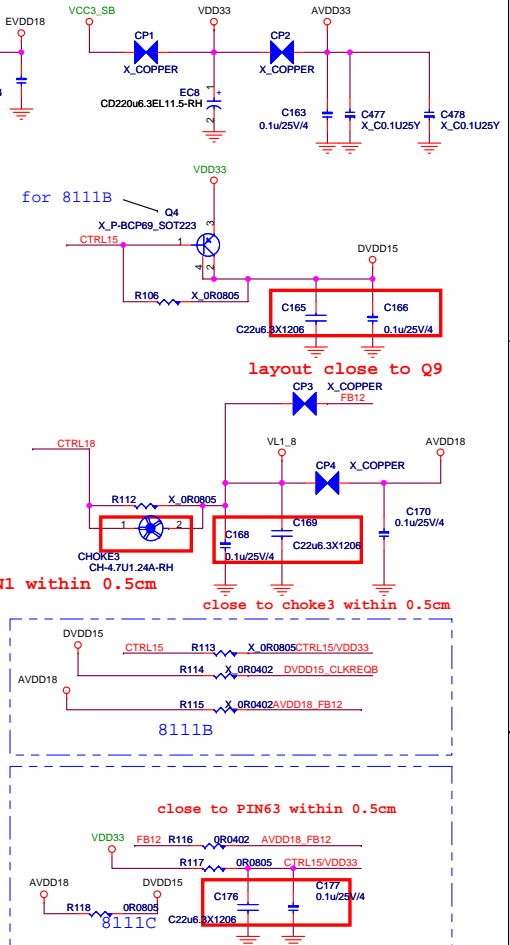
PCI PULL-UP / DOWN RESISTORS









| | RTL8111B / RTL8101E | RTL8111C | |
|--------|------------------------|----------|--|
| AVDD33 | 3.3V | 3.3V | |
| AVDD18 | 1.8V | 1.2V | |
| EVDD18 | 1.8V | 1.2V | |
| DVDD15 | 1.5V | 1.2V | |
| | | | |

| | Q9 | Q10 |
|----------|-------------|-------------|
| RTL8111B | <i>Need</i> | <i>Need</i> |
| RTL8111C | <i>N/A</i> | <i>N/A</i> |



| Power consumption | | |
|-------------------|-------|------|
| | 1G | 100M |
| 3.3V | 103mA | TBD |
| 1.5V | 367mA | TBD |
| 1.8V | 198mA | TBD |

-16F0031-P02

| Giga-Lan | | 10/100-Lan | |
|-----------------|---|------------------------------------|---|
| N58-22F0181-S42 | | N58-22F0061-S42 N58-22F0061-F02 | |
| Link | Yellow | Link | Yellow |
| Active | Blinking | Active | Blinking |
| 1000 | Orange | 100 | Green |
| 100 | Green | 10 | None |
| 10 | None | | |
| 19 |  | 19 |  |
| 20 | Yellow | 20 | Yellow |
| 21 |  | 21 |  |
| 22 | Green | 22 | Green |



Video Connector

Power 20 mils

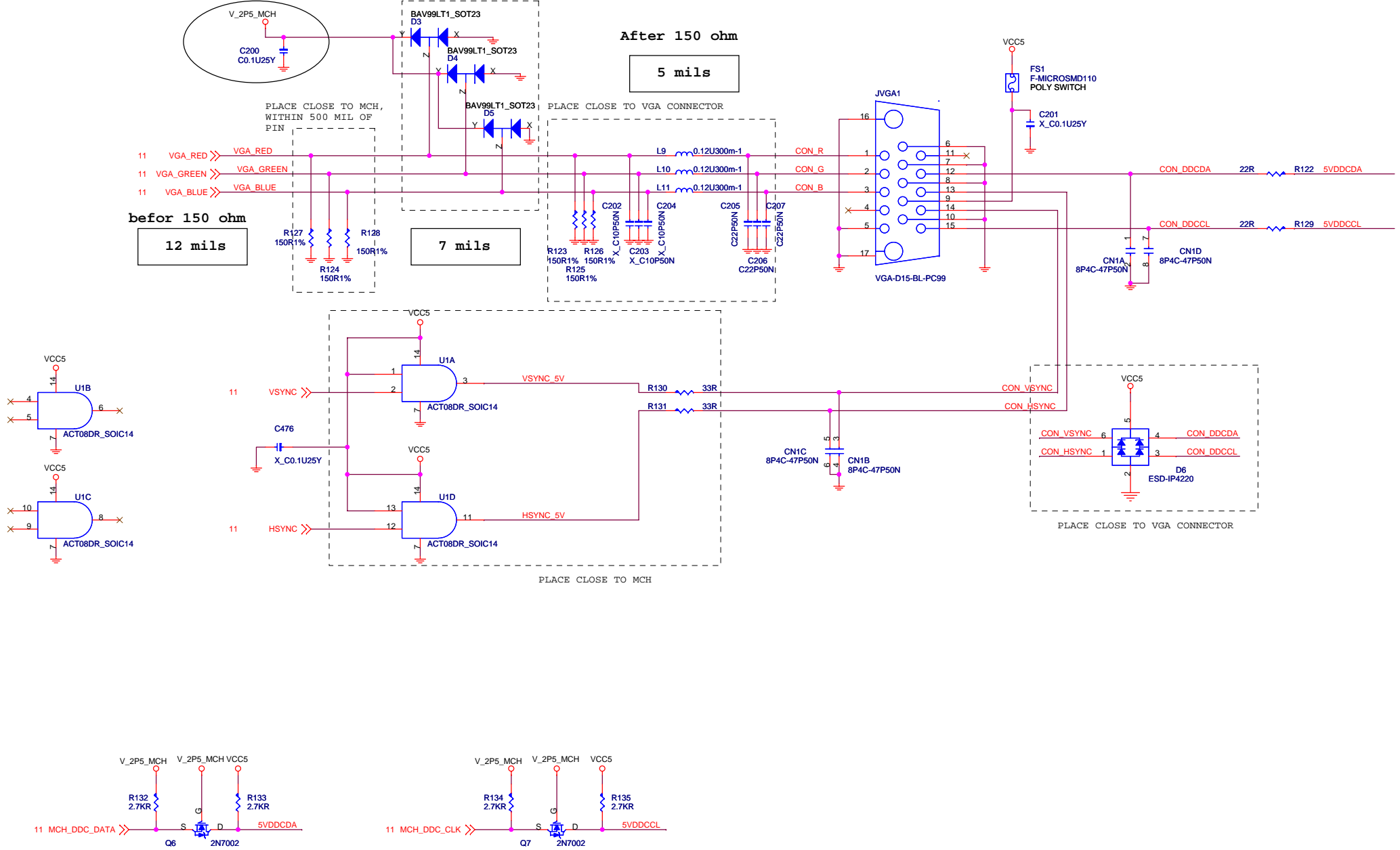
After 150 ohm

5 mils

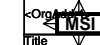
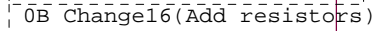
before 150 ohm

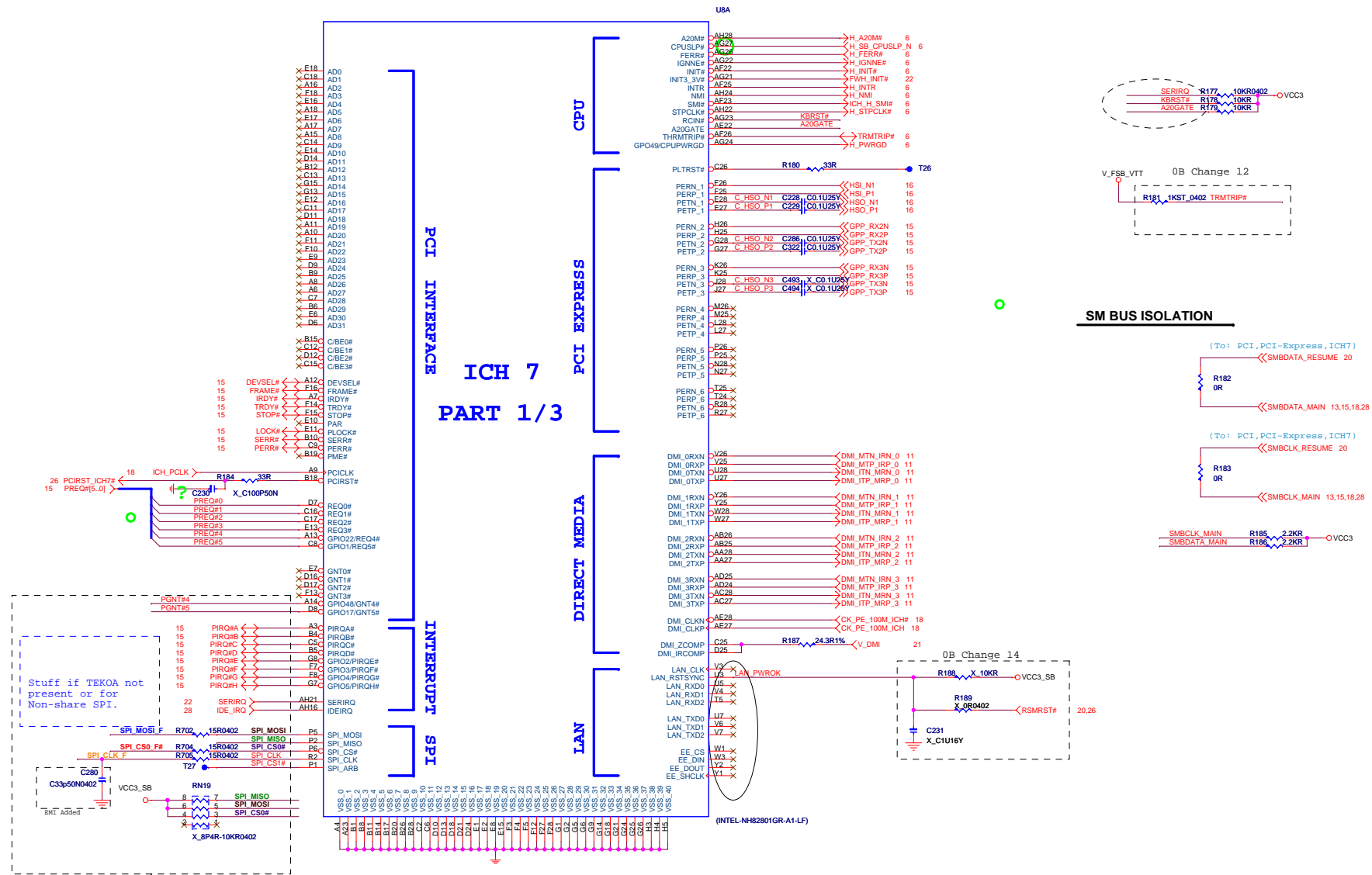
12 mils

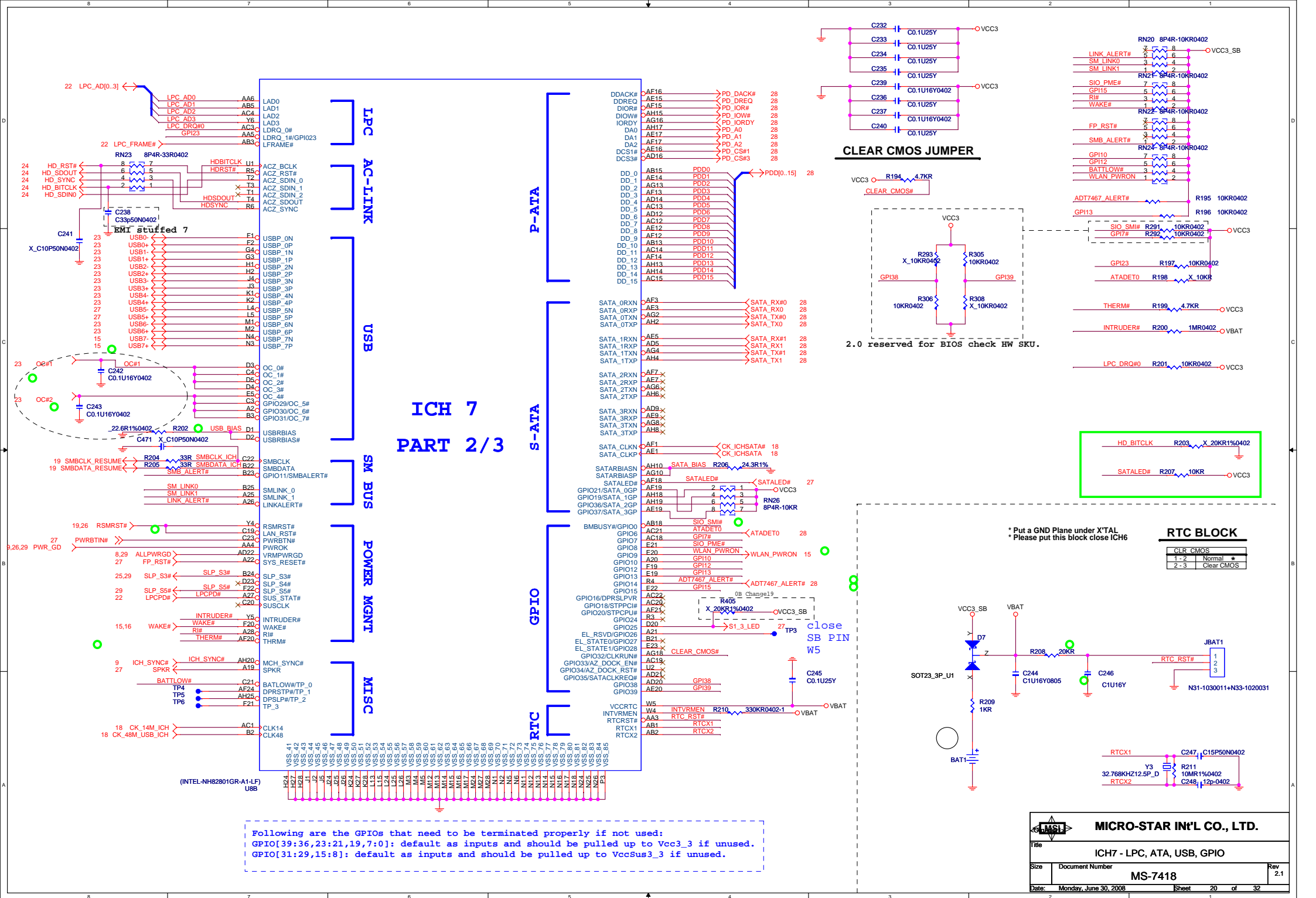
7 mils

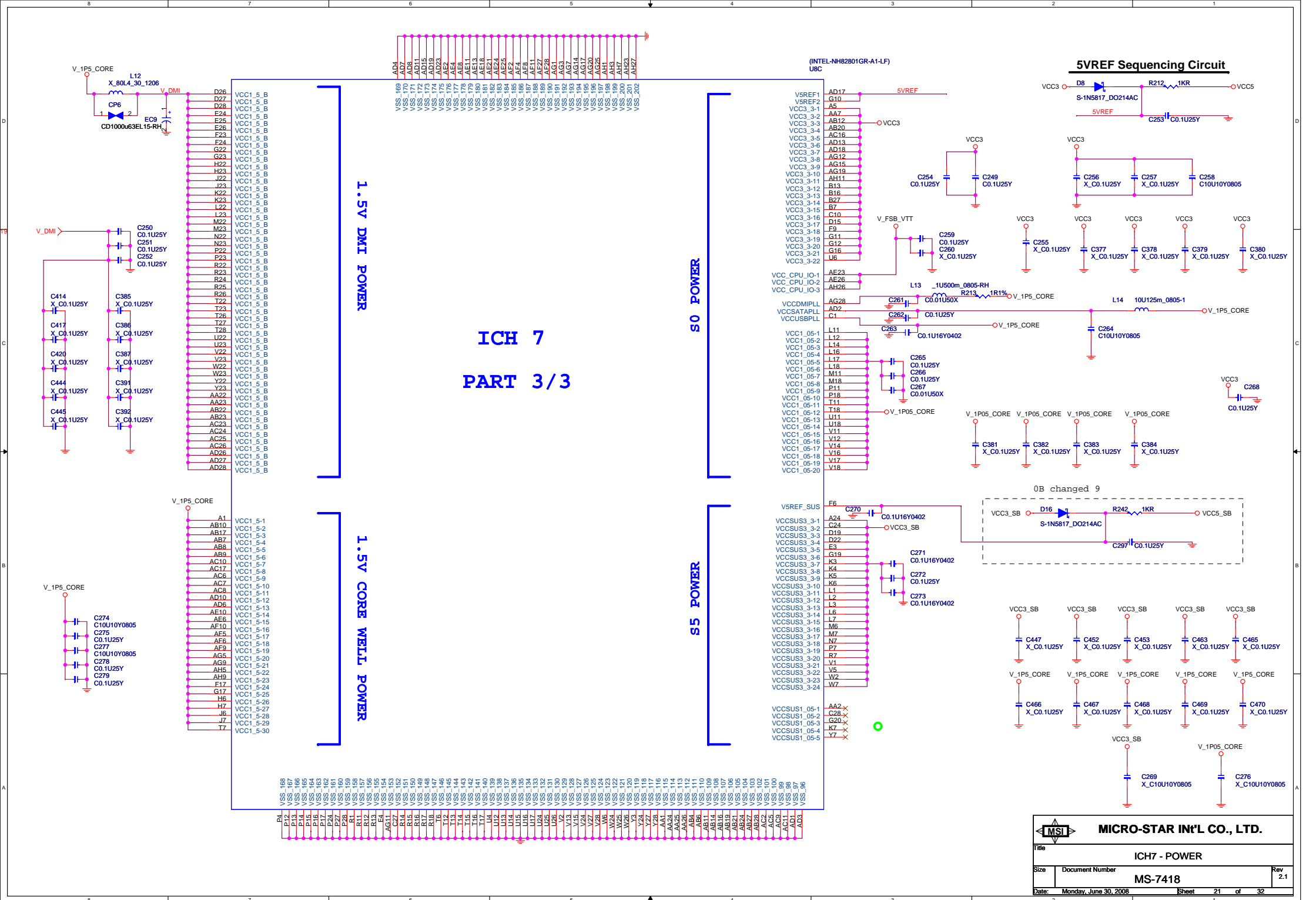


Trace length less than 0.5inches

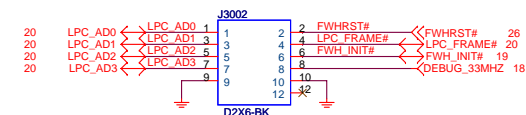




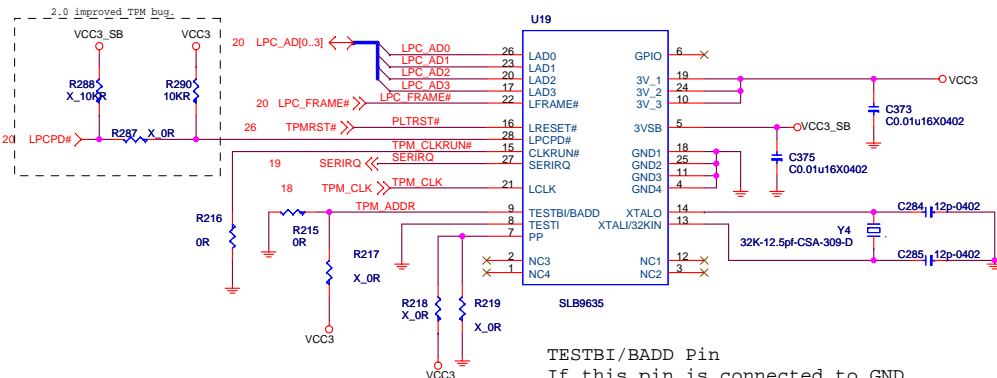




LPC Debug Port

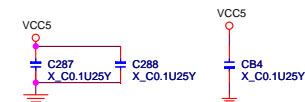
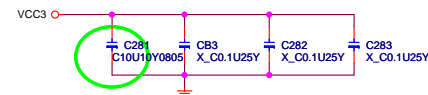


IO Address: 0x02E



TESTBI/BADD Pin

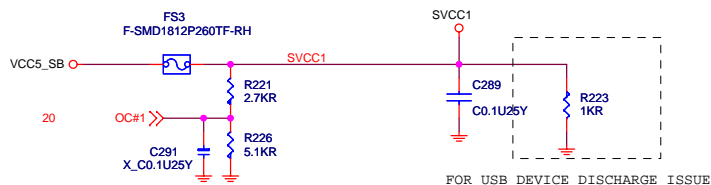
If this pin is connected to GND,
addresses 2EH/2FH are used.
If it is strapped to VCC,
addresses 4EH/4FH are used.



MICRO-STAR INT'L CO., LTD.

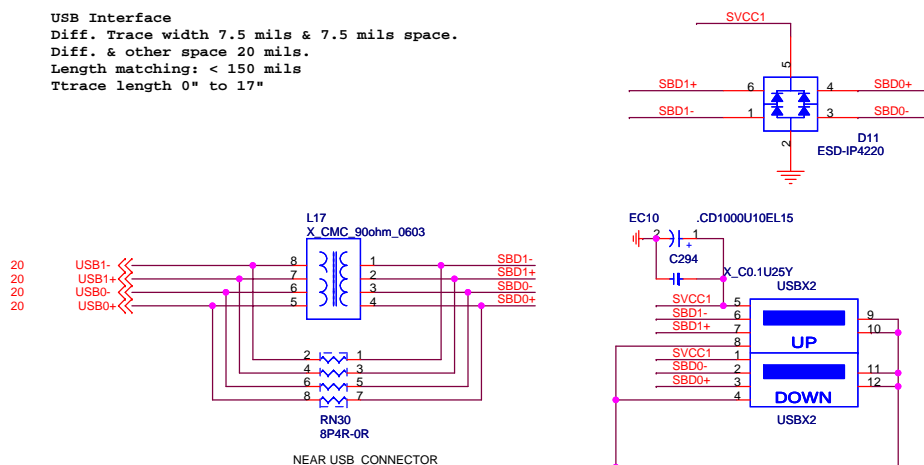
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|-------|-----------------------|---------|----------|
| Title | | FWH | |
| Size | Document Number | MS-7418 | |
| Date: | Monday, June 30, 2008 | Sheet | 22 of 32 |
| | | Rev | 2.1 |

POWER CIRCUIT FOR USB PORT 0,1,2,3 (REAR)



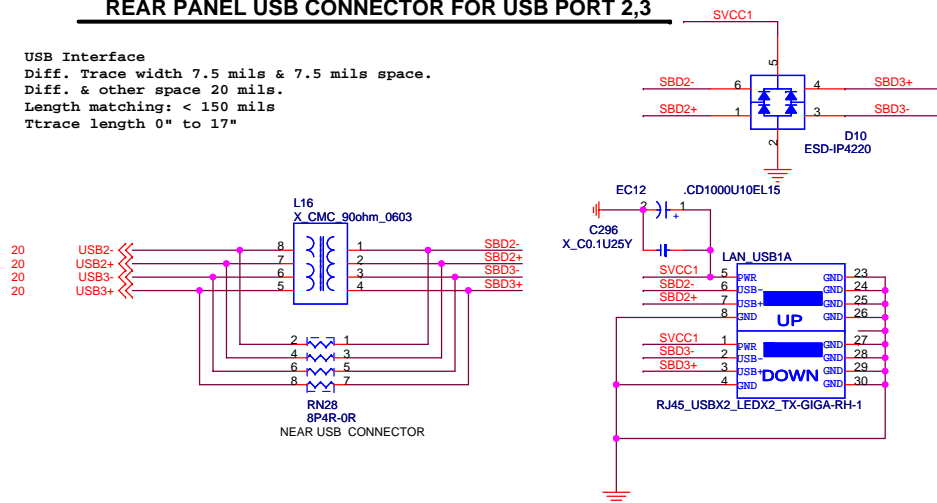
REAR PANEL USB CONNECTOR FOR USB PORT 0,1

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

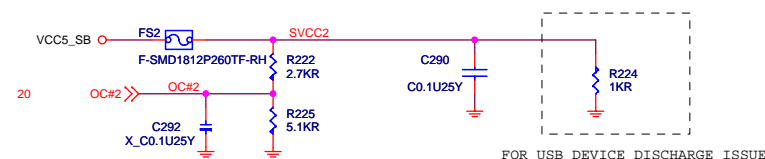


REAR PANEL USB CONNECTOR FOR USB PORT 2,3

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

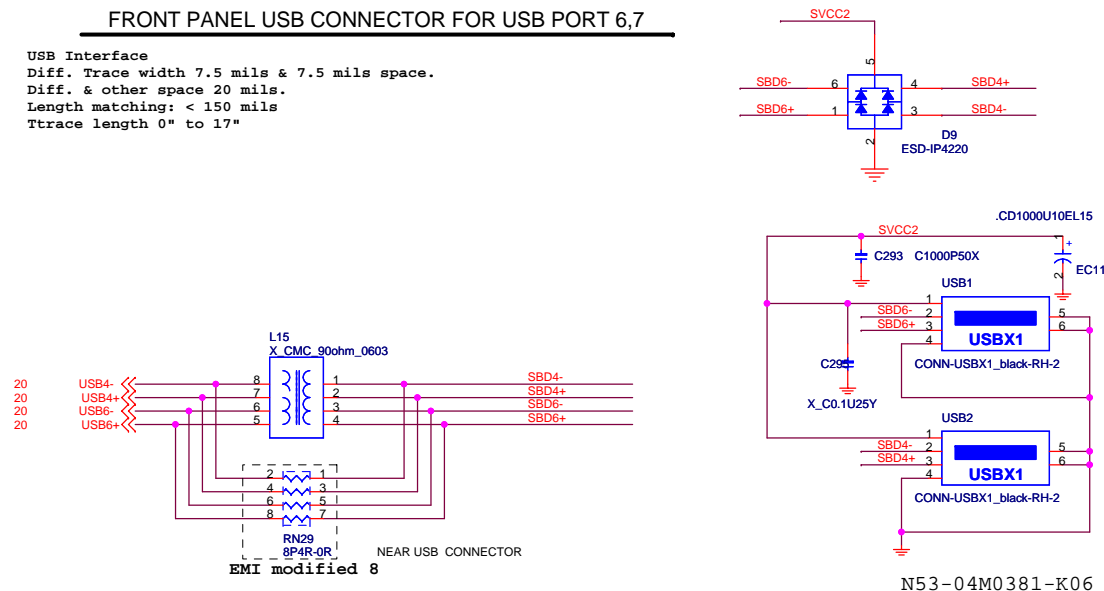


POWER CIRCUIT FOR USB PORT 4,6,7 (FRONT)



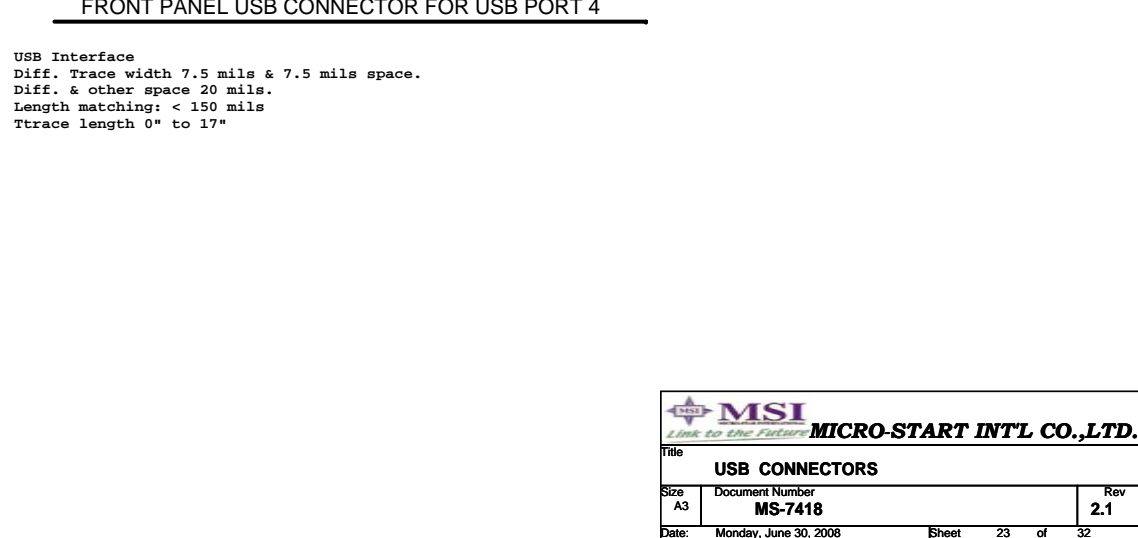
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

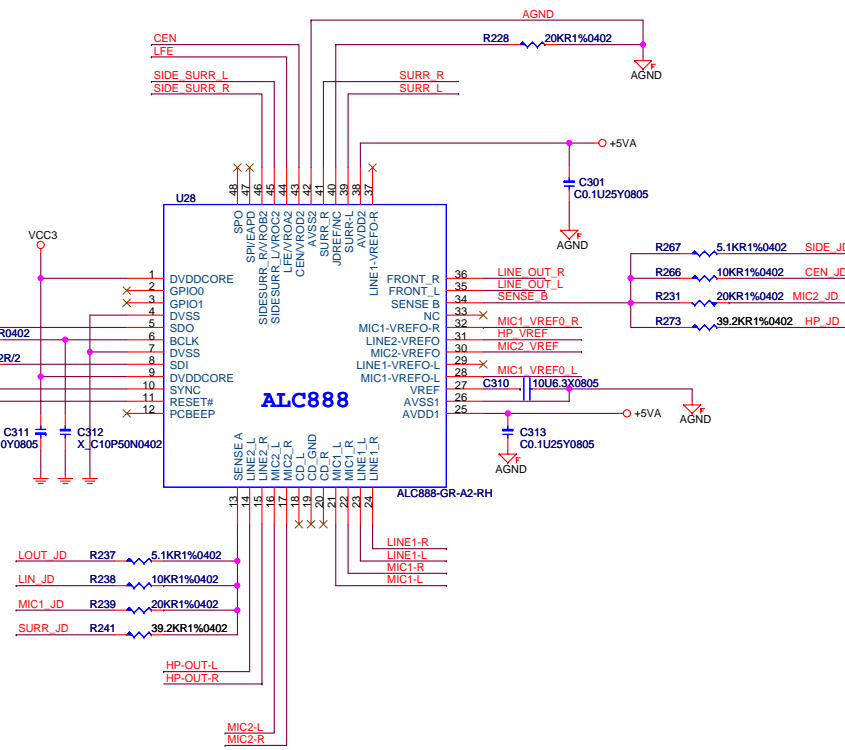


FRONT PANEL USB CONNECTOR FOR USB PORT 4

USB Interface
Diff. Trace width 7.5 mils & 7.5 mils space.
Diff. & other space 20 mils.
Length matching: < 150 mils
Trace length 0" to 17"

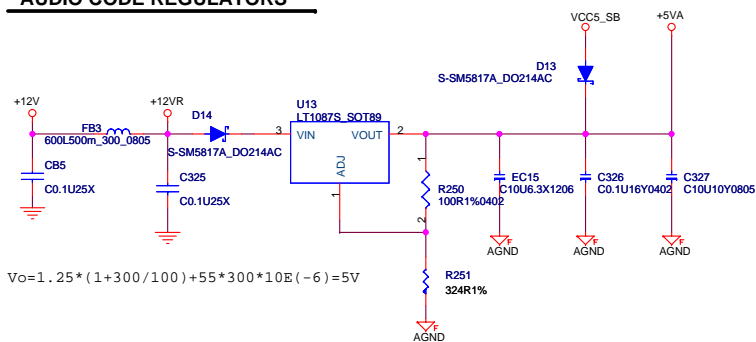


ALC888



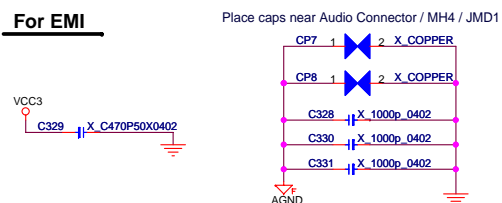
Trace length less than 0.5inches

AUDIO CODE REGULATORS

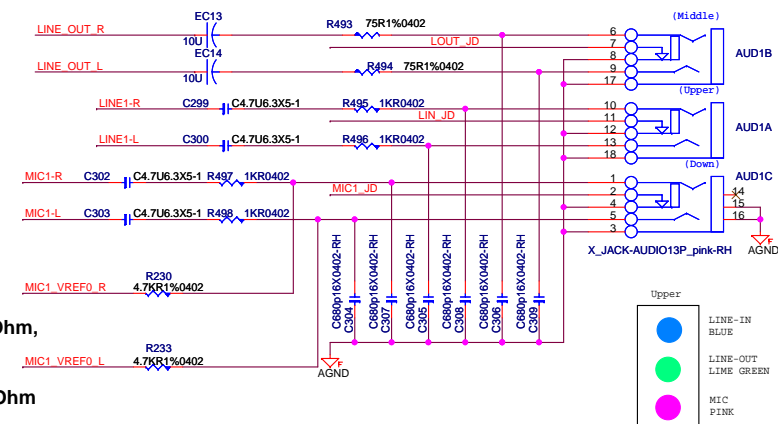


$$V_o = 1.25 * (1 + 300/100) + 55 * 300 * 10E(-6) = 5V$$

For EMI

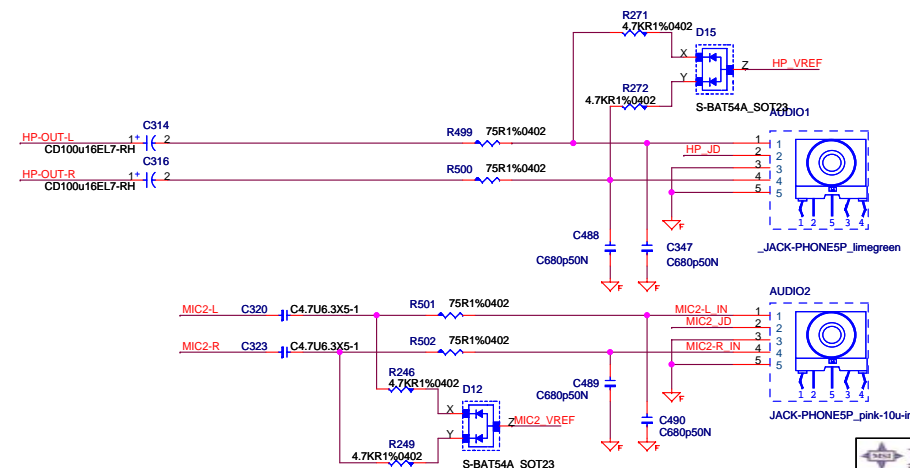
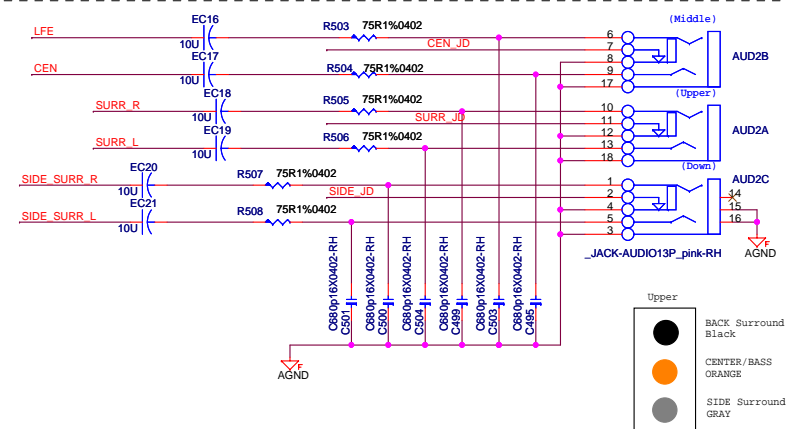


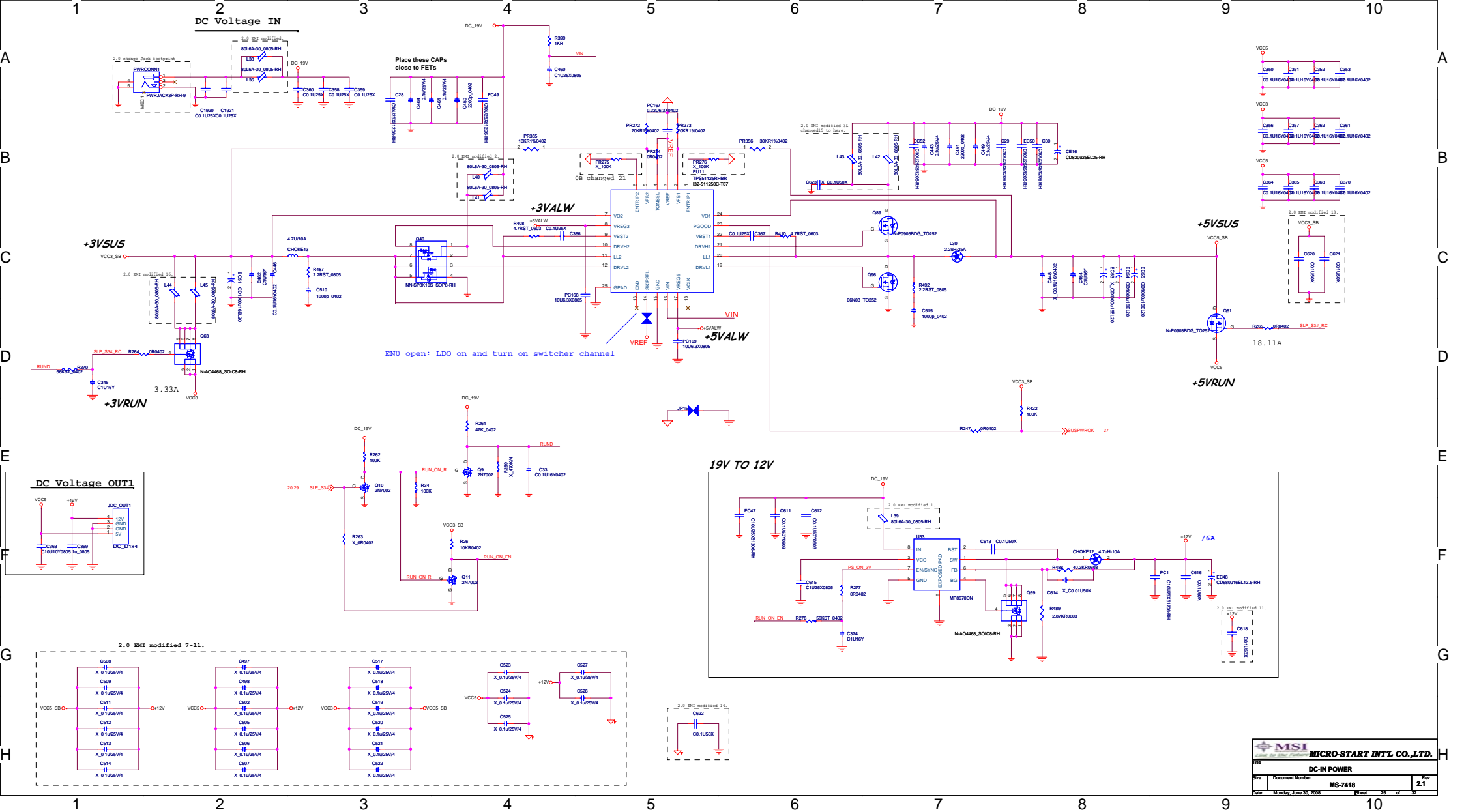
PHONE JACKER (HDA JACK)

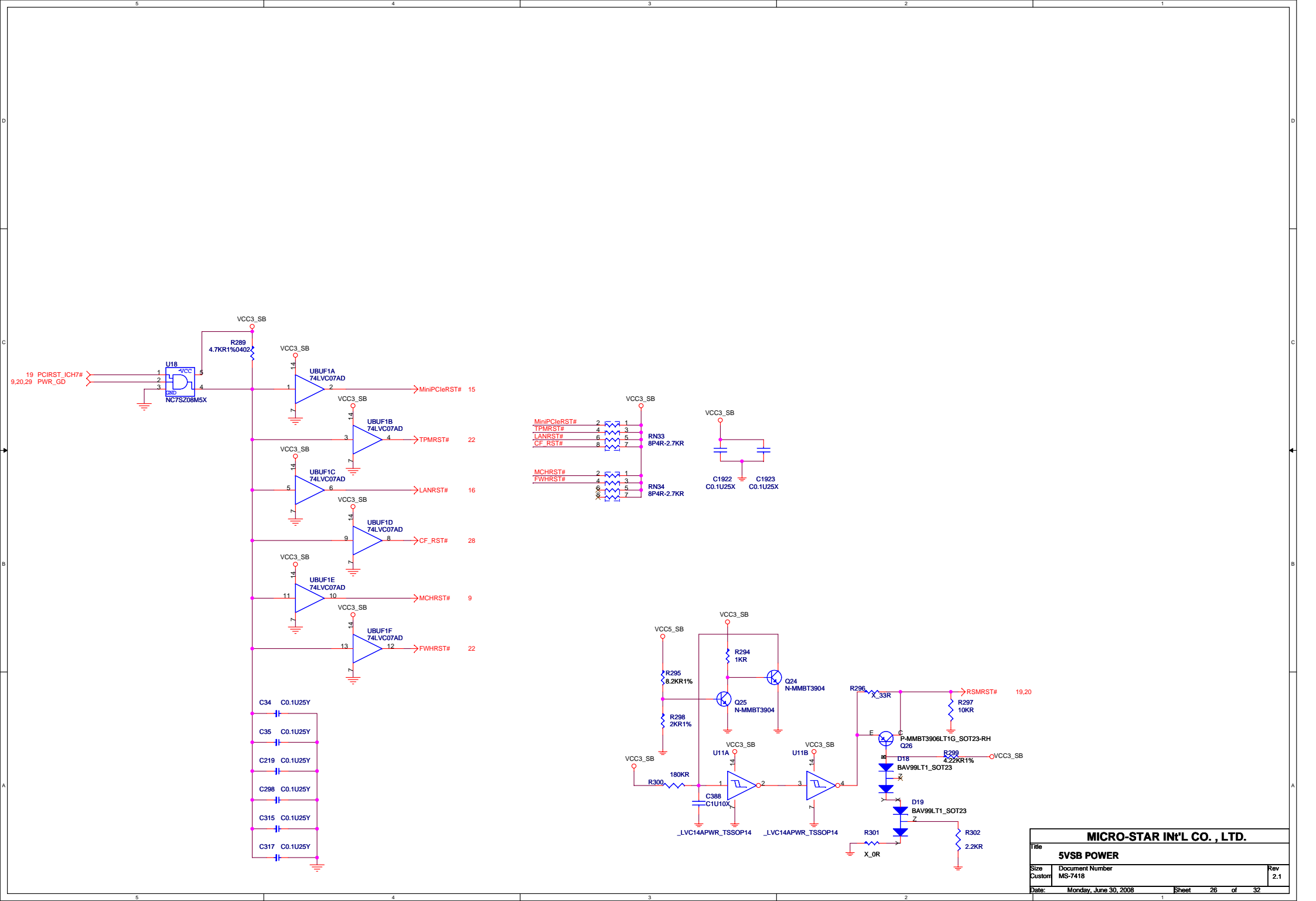


5.1 ch-->N54-13F0171-S42
R495&R496&R497&R498 =75 Ohm,

7.1 ch-->N54-26F0111-K06
R495&R496&R497&R498 =1K Ohm

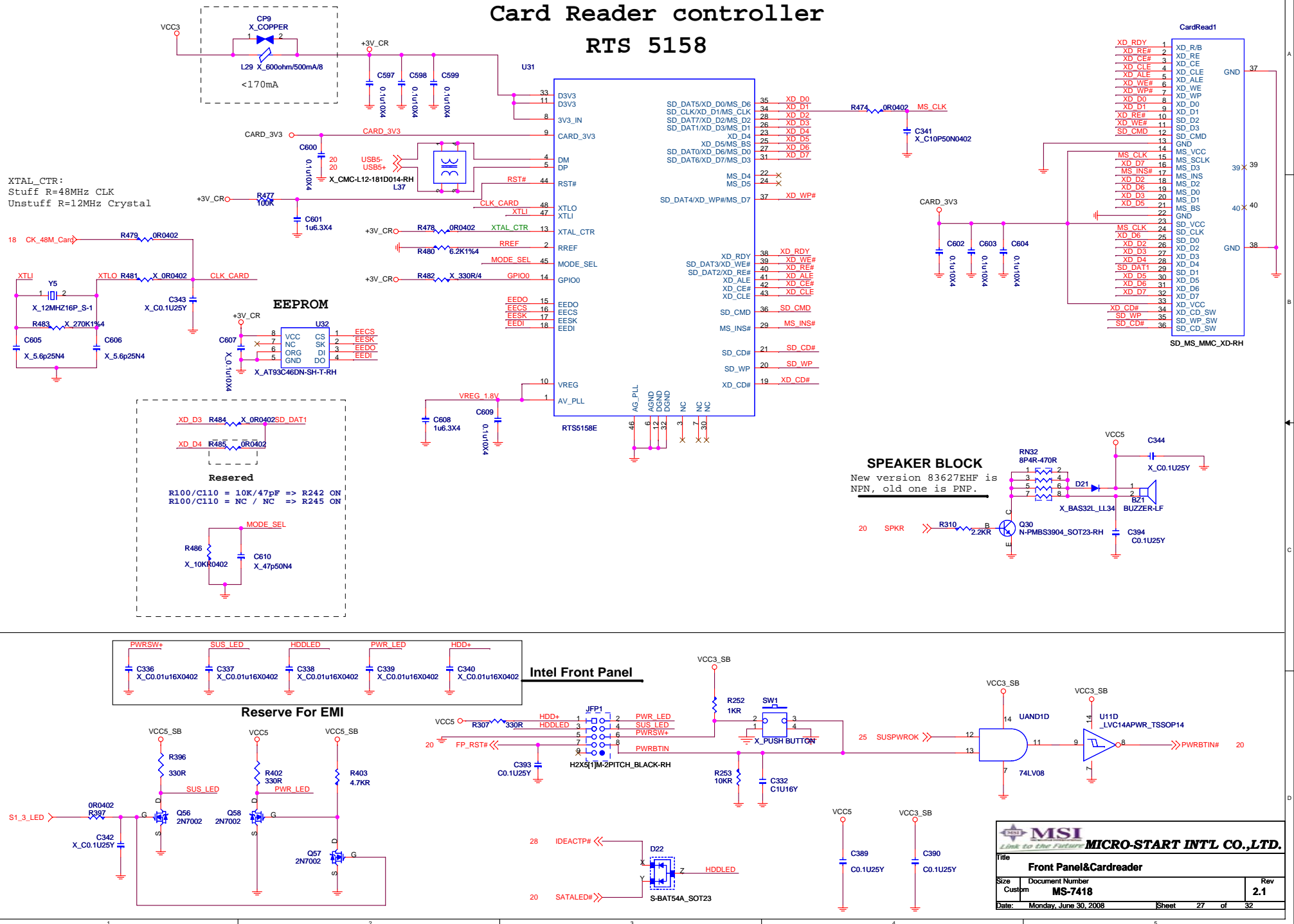




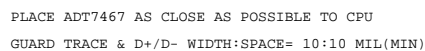
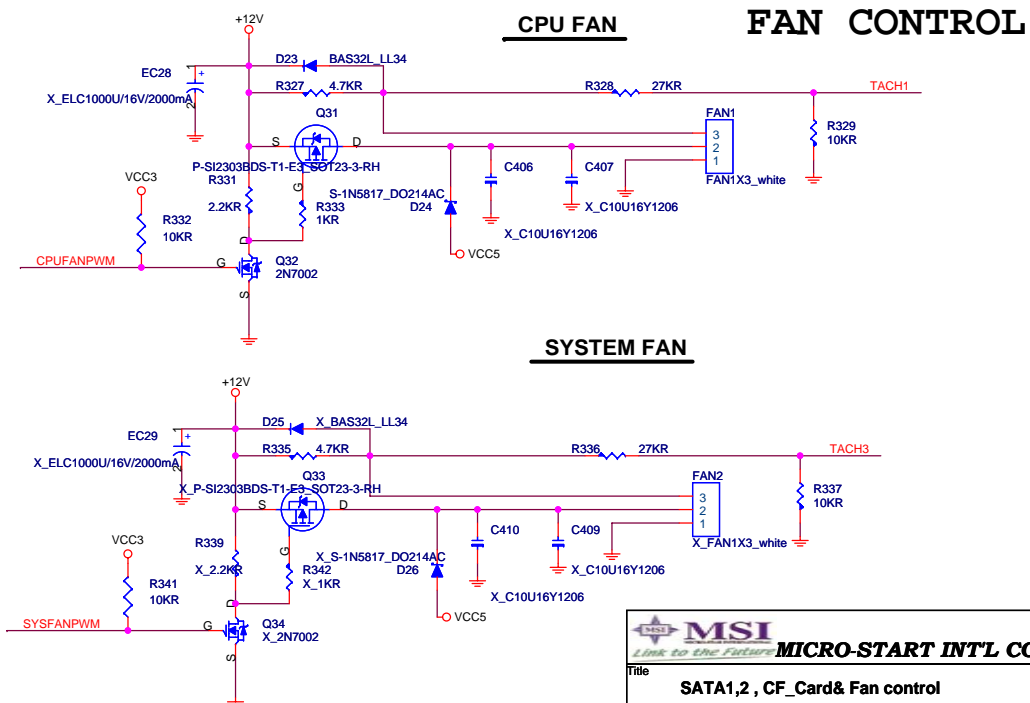
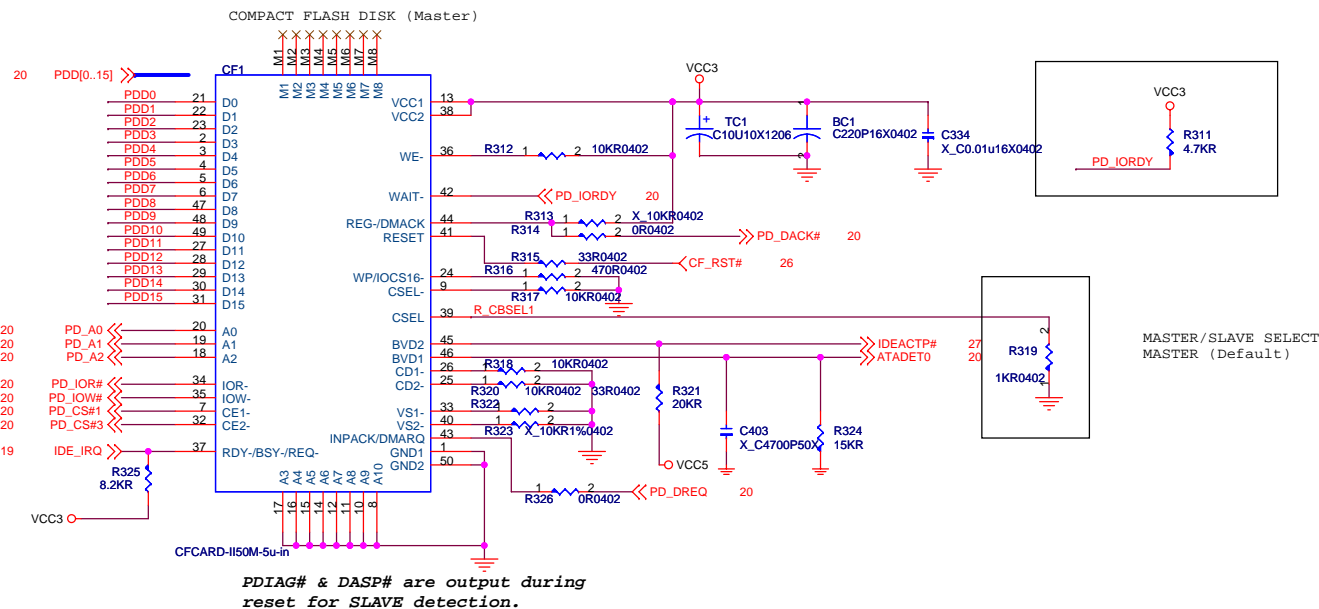


Flash Card Socket

Card Reader controller RTS 5158



COMPACT FLASH CONNECTOR



ACPI Controller

DDR2 1.8V POWER...7.95A

Internal reference $V_{fb}=0.6V$ (+/- 1.5%)
Better than external reference (+/-5%)
==>Using Stand-alone mode

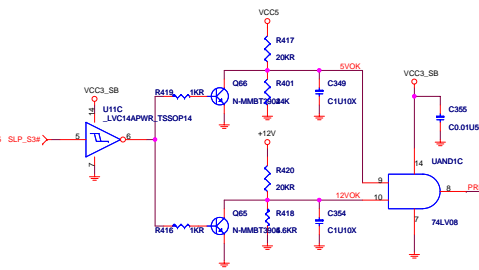
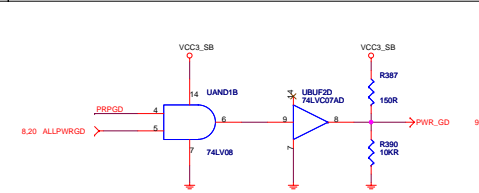
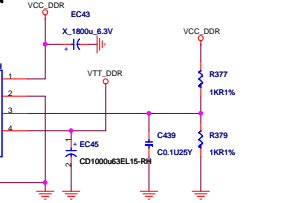
$$V_{fb}=V_{out} * [1.5 / (1.5 + 3.01)] = 0.6V \quad V_{out} = 1.804V$$

DDR2 1.5V POWER...22.84A

$$V_{fb}=V_{out} * [2 / (2 + 3.01)] = 0.6V \quad V_{out} = 1.503V$$

VTT1.1V POWER...4.9A

DDR VTT Power

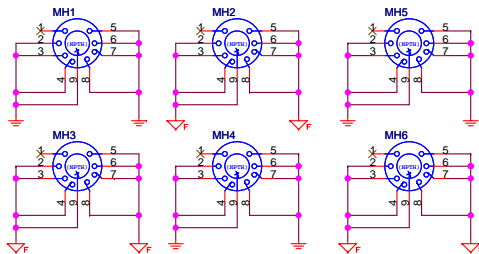


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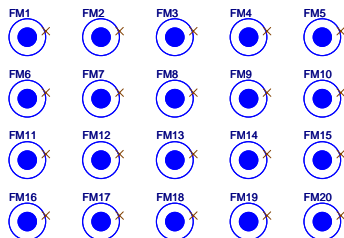
MS7 ACPI CONTROLLER
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Auto-BOM Manual Parts

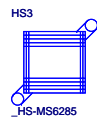
Mounting Holes



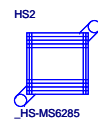
Optics Orientation Holes



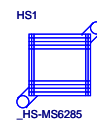
CPU HEAT SINK



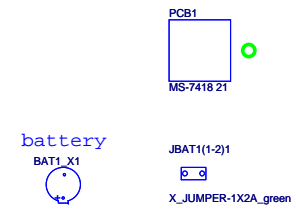
NB HEAT SINK



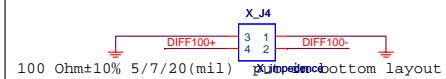
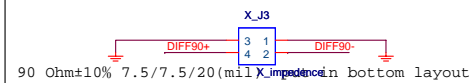
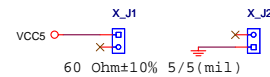
SB HEAT SINK



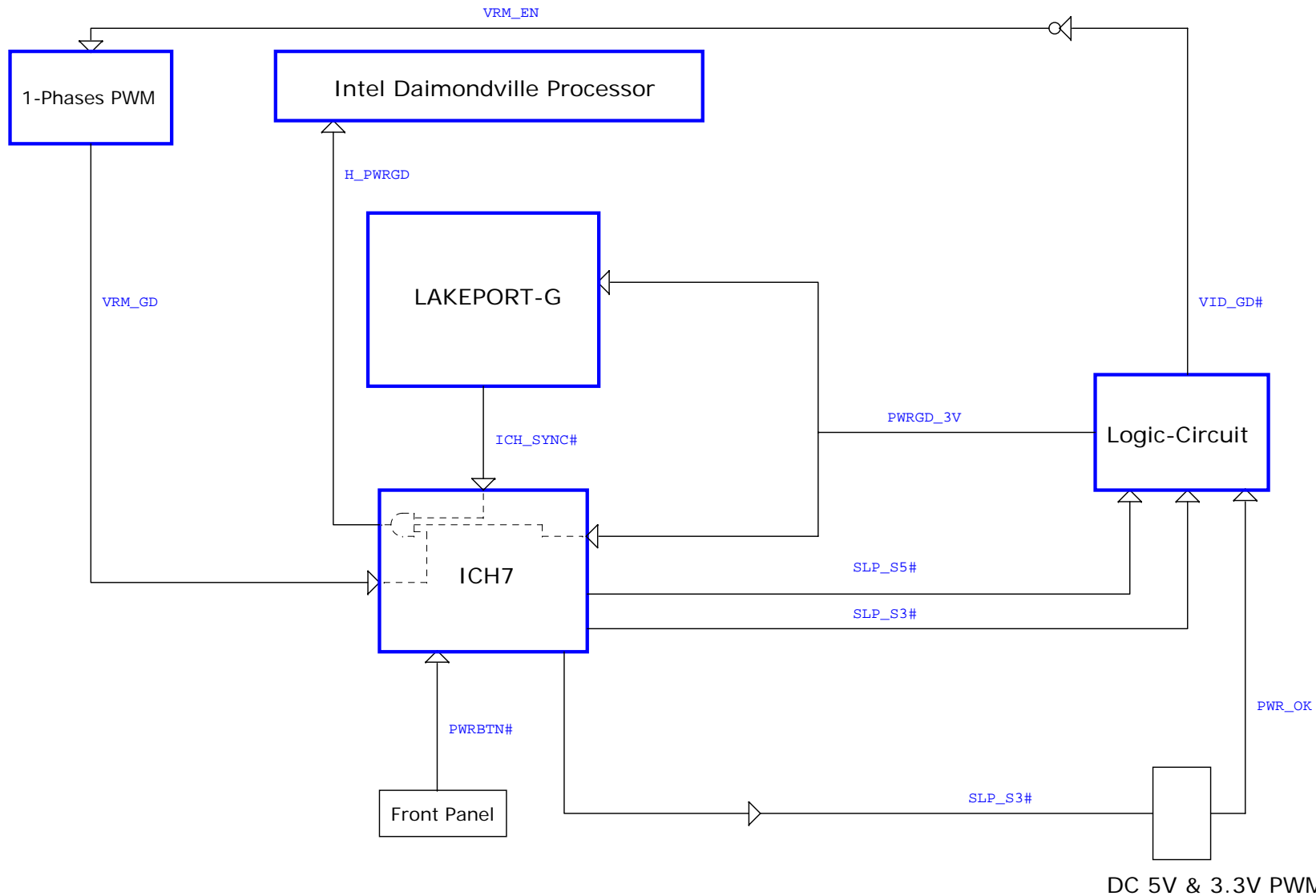
MANUAL PART




Simulation



PWROK MAP



| | | | |
|---|-----------------------|----------------|---------|
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| Title | | PWOK MAP | |
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0B changed 1-->Pull up follow design guide.(page6)
0B changed 2-->Pull up follow design guide.(page6)
0B changed 3-->Pull up follow design guide.(page6)
0B changed 4-->Pull up follow design guide.(page6)
0B changed 5-->Pull up follow design guide.(page6)
0B changed 6-->Change R4,R8 to 24.9R, R6,R9 to 49.9R. (page6)
0B changed 7-->unstuff R304,stuff R303 follow CRB V0.7.(page7)
0B changed 8-->-->change pull up circuit follow CRB V0.7.(page7)
0B changed 9-->make sure the power sequence.(page21)
0B changed 10-->improve the "PWR_GD" single waveform negative pulse issue. (page8)
0B changed 11-->improve the "VRM_GD","ALLPWRGD" single waveform pulse issue. (page29)
0B changed 12-->Change resistor value follow design guide.(page19)
0B changed 13-->Pull up follow design guide.(page6)
0B changed 14-->unstuff R188 follow CRB V0.7.(page19)
0B changed 15-->Add SPI Bios interface and strapping resistor. Add PCI interface.
0B changed 16-->Add pull down Resistors.(page18)
0B changed 17-->Change EC28 same as EC29 for mechanical issue.(page28)
0B changed 18-->Change R176 from 5.6k to 1k and change Q8 from 3904 to 2N7002 for UBUF2's pin11 voltage level drop to 2V issue.(page18)
0B changed 19-->unstuff R405 for GPIO25.(page20)
0B changed 20-->Connect MCHREF voltage to SMVREF0 and SMVREF1.(page10)
0B changed 21-->Unstuff PR275,PR276 for no standby power issue.(page25)
0B changed 22-->Reserve test point on MCH H_A#32~H_A#35 (page9)
0B changed 23-->Remove FWH BIOS interface(page22)
0B changed 24-->Change 19V to 12V circuit.(page25)
0B changed 25-->Change CPU part number to A09-1320165-I06 (page 6&9)
0B changed 26-->Stuff TPM circuit for BIOS bring up(page 22)
0B changed 27-->Unstuff MiniPCIE2 circuit(page 15)
0B changed 28-->Change CPU,NB,SB heatsink footprint(page 30)
0B changed 29-->Change MIC1,HP-OUT Vref circuit(page 24)
0B changed 30-->Change VID circuit for jump VID and add 4pcs 10u cap.(page7,8)
0B changed 31-->Change choke11 material(page29)
0B changed 32-->Add 6 pcs 0.1uF caps for EMI issue(page26)
0B changed 33-->change LAN chip from VBO to VCO version.

2.0 change:
EMI Modified circuit.
1. add L02-8008074-J07 at U33 pin 8 (DC_19V)
2. add L02-8008074-J07 *2 at Q40 pin 1,2 (DC_19V)
3. add L02-8008074-J07*2 at Q89 pin D (DC_19V)
4. 預留 cap 0603 104pF *1 at Q47 pin D (V_1P5_CORE)
5. 預留 Resister 0805 0ohm *2 at Q63 pin 5,6,7,8 (VCC3_SB)(取消此變更)
6. 預留 snubber RC 2.2R+1000pF at CHOKE9 pin 1
7. 預留 moat cap 104pF*6 (+12V to VCC5)
8. 預留 moat cap 104pF*6 (+12V to VCC5_SB)
9. 預留 moat cap 104pF*6 (VCC5_SB to VCC3)
10. 預留 cap 104pF*3 (VCC5 to AGND)
11. 預留 cap 104pF*2 (12V to AGND)
12.change C304、C305、C306、C307、C308、C309、C347、C488、C489、C490、C495、C499、C500、C501、C503、C504 to 680pF (Audio out)
13. change L36、L38 to L02-1218034-C08(取消此變更)

2.1 change: Shift JDC_OUT1 4mm for mechanical issue and add customer consign material.


0B changed 34-->
VCCP
1. R40: 14.7k ohm (droop) 2. C24: 0.022uF (RC)
3. R42: 24k ohm (RC) 4. R45: 487 ohm (OCP)
5. R50: 22k ohm (comp) 6. C37: 0.1uF (comp)
7. C22: no pop
VCC_DDR
1. R350: 3.09k ohm (offset) 2. R354: 1.54k ohm (offset)
V_1P5_CORE
1. CHOKE11: L04-11A7231-W15

0B to 0C change:
1. Change page25 19V to 12V 2. Add C1920~C1923
3. Modify FAN control sch 4. change R399 to 1k For the AC ON/OFF issue
5. EC53不上件,EC51,EC54,EC55改為C94-1021671-P01
6. EC48改為C94-6811621-N10

0C change:
stuff C14 for lost USB controller issue.
unstuff C407 for FAN voltage not linear issue.

1.0 change:
1.Add EMI "BOM" solution.
(1).add C472 33pF (CK_48M_CARD)
(2). add C216 10pF (CK_48M_USB_ICH)
(3). add C221 33pF (TPM_CLK)
(4). add C212 10pF (ICH_PCLK)
(5). add C348 33pF (DEBUG_33MHZ)
(6). add C189 104pF (N19033424)
(7). add C238 33pF (HD_BITCLK)
(8). change RN29 to L12-1218027-CA8 (USB4 & USB6)
2.unstuff FAN2 circuit.
3.change DC Jack to new part N92-03M0391-H06.
4.unstuff SW1.

2.0 change:
14.change power Jack footprint to new material N92-03M0391-H06
15.disconnect "LPCPD#" pull high to VCC3_SB and add R287,R288,R290 but only stuff R290.
16.removed RN25 and add R291,R292,R293,R305,R306,R308 but only stuff R291,R292,R293,R305.
for BIOS check PCB SKU.
17.add C159
18.C448 不上件
19. add cap 0603 104pF *1 (+12V to GND)
20. add cap 0603 104pF *1 at MINI_PCIE2 pin 1(WAKE#)
21. add cap 0603 104pF *2 (VCC3_SB to GND)
22. add cap 0603 104pF *1 (GND to AGND)
23. 預留 cap 104pF*1 at L30 左邊 (N47600954 to GND)
24. add L02-8008074-J07*2 at Q63 pin5,6,7,8 (VCC3_SB)
25.disconnect UBUF2 pin14 of partA-E
and add voltage divided circuit at part E.
26.Add C280 for EMI.
27.EMI modify C1916 connect between VCC5 and GND
for SPI clock.
28.change BOM for PCB version detection.

| | | | |
|---|-----------------------|----------------------------|----------------|
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| Title History | | | |
| Size | Document Number | | Rev |
| | MS-7418 | | 2.1 |
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